GOEPEL electronic focuses boundary scan platform toward embedded system access technologies

GOEPEL electronic recently demonstrated the series version 4.6 of its Boundary Scan software platform SYSTEM CASCON holistically supporting all Embedded System Access (ESA) technologies.

The new release fundamentally extends the software platform's focus towards the overall paradigm change to non-intrusive test and programming procedures. Therefore, SYSTEM CASCON was complemented by a series of basically new system tools and features in particular for holistic development, validation and execution of ESA projects.

"What started with Boundary Scan 20 years ago, today presents as a team of more than a dozen complementary technologies for Embedded System Access. With our enhanced software platform we are the first vendor being able to unite the entire potential of these innovative test and programming strategies into a completely integrated and organically grown environment", says Thomas Wenzel, Managing Director of GOEPEL electronic's JTAG/Boundary Scan Division. In contrast to other vendors, we put particular emphasis to extraordinary integration and interaction opportunities to the classic intrusive methodologies such as In-Circuit-Test or Flying Prober, providing our customers an additional value in test quality by combination solutions. This philosophy gives us a top position in regards to the on-going paradigm change."

SYTEM CASCON V 4.6 exploits the integrated features for adaptive access management, process automation as well as graphical project development for all relevant ESA technologies. In addition to IEEE 1149.x, particular targets are Processor Emulation Test (PET), FPGA Assisted Test (FAT), Core Assisted Programming (CAP), FPGA Assisted Programming (FAP) and Chip Embedded Instrumentation. Utilising a special dynamic data management enables a real fusion between the single technologies during the operation – additional interactive operations are possible. For example, specific guarding conditions can be created on the unit under test (UUT) per Boundary Scan. This is the precondition to a targeted application of chip embedded instruments controlled by ChipVORX. The solution's necessary openness is achieved by an independent model library for component description, processor IP and FPGA IP. It consistently follows the principle of software reconfigurable instrumentation up to hardware level.

SYSTEM CASCON is a professional JTAG/Boundary Scan development environment, developed by GOEPEL electronic with currently 47 completely integrated ISP, test, and debug tools for design validation, production test as well as field service. Regarding the hardware, SYSTEM CASCON is ideally supported by several controllers such as PicoTAP, elements of the SCANBOOSTER family, as well as by

the hardware platform SCANFLEX.

The shipping of SYSTEM CASCON 4.6 has already started, being free-of-charge for customers with valid maintenance contract.

Further information about the company and its products can be found on the internet at www.goepel.com [1].

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[1] http://www.goepel.com