

28-nm Multi-Gear M-PHY IP Supports Six Standards for Mobile Apps

Synopsys, Inc. announced availability of a new DesignWare MIPI M-PHY IP solution supporting multiple speed gears and a broad range of high-speed interfaces for mobile applications. Based on the first DesignWare MIPI M-PHYSM IP introduced by Synopsys in 2010, the new MIPI M-PHY IP is said to be the first 28-nanometer (nm) multi-gear solution that supports six different inter-chip interconnect protocols including the JEDEC Universal Flash Storage (UFS), the USB SuperSpeed Inter-Chip (SSIC), and the MIPI Alliance's Low Latency Interface (LLI), DigRF v4 and future CSI-3 and DSI-2 interfaces. By providing application-oriented M-PHY IP that runs at multiple speeds and is interoperable with multiple protocols, teams can "future-proof" their designs, according to the company, while reducing the risk and cost of integrating MIPI interfaces into basebands, application processors and mobile ICs.

The 28-nm DesignWare MIPI M-PHY IP offers Type-I and Type-II low-speed implementations to support different application requirements. With support for high-speed GEAR1, GEAR2 and GEAR3, ranging from 1.248 Gbps to 5.8 Gbps, this scalable solution can meet ever-increasing data rate requirements, enabling reuse of proven IP in next-generation devices. Using a variety of high-speed and low-speed burst modes and power management modes, including idle, sleep and hibernate with quick entry and exit capability, Synopsys' DesignWare MIPI M-PHY IP can be optimized to achieve required data rates while meeting the stringent power and area requirements of mobile SoCs.

The DesignWare MIPI M-PHY IP is compliant with the MIPI Alliance M-PHY v1.0 specification. By working closely with the MIPI Alliance to develop its specifications, Synopsys targets its IP to comply with future MIPI M-PHY specification releases. Synopsys DesignWare MIPI M-PHY IP supports High Speed GEAR1, GEAR2 and GEAR3 rates A/B along with Type-I and Type-II low-speed capabilities. The DesignWare MIPI M-PHY's modular architecture allows implementation of a variety of transmitter and receiver lanes to meet a broad range of system requirements and all modes outlined in the protocol specification. A sophisticated clock recovery mechanism and power efficient clock circuitry are designed to maintain the integrity of the clocks and signals required to meet strict timing requirements. The DesignWare MIPI M-PHY supports large and small amplitudes, slew rate control and dithering functionality for optimized electromagnetic interference (EMI) performance.

The multi-gear DesignWare MIPI M-PHY IP in the 28-nm process node will be available for early adopters in calendar Q2, 2012.

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