

Virage Logic Introduces MIPI D-PHYs and Controllers on 40LP Process

Virage Logic Corporation (NASDAQ:VIRL), the semiconductor industry's trusted IP partner, today announced the availability of its SiPro™ MIPI Rx D-PHY and MIPI Tx D-PHY as well as CSI Rx (camera serial interface receiver) and DSI Tx (display serial interface transmitter) controllers on the 40LP process node in Q2 of this year which are based on the production proven D-PHYs announced last year. Virage Logic's production proven SiPro MIPI CSI and DSI D-PHYs and controllers are immediately available on the 65LP process node. Development costs for such complex MIPI PHY SERDES typically run higher than 40 man-years. Virage Logic's SiPro MIPI Rx D-PHY and Tx D-PHY solutions are system-on-chip (SoC) verified and fully compliant with the latest D-PHY v1.00 MIPI standard. Shipping in a mobile device for over a year, the production proven SiPro MIPI Rx D-PHY and Tx D-PHY has been proven to consume the lowest power with minimum silicon area and significantly reduced design risk. Specially architected for a faster improvement in chip yield, the IP solution expedites volume ramp-up to ensure maximum production success.

"Compared to alternative bi-directional solutions on the market, the SiPro MIPI solution provides 70 percent area savings, 80 percent lower power consumption, approximately 20 percent better performance and high yields through yield-calibration circuitry," said Kamalesh Ruparel, vice president and general manager of Virage Logic's ASIP Solutions Group. "With Virage Logic's industry leading production proven technology on advanced process nodes and its optimized characteristics, customers get to market faster while meeting stringent power and silicon cost budgets."

"The MIPI interface will do well," said Will Strauss, President of Tempe, AZ-market research firm Forward Concepts. "With the major semiconductor players, such as Texas Instruments on its upcoming OMAP 4 chip and ST Micro as a major Nokia chip supplier, beginning to incorporate the interface on their devices, the market should grow nicely."

About Virage Logic's SiPro MIPI IP

The SiPro MIPI DSI (display serial interface), CSI (camera serial interface) controllers and D-PHY IP are optimized for power, area, yield and performance. The SiPro MIPI IP was system-validated with device ICs to provide seamless interoperability for evolving mobile electronics applications interfacing cameras and displays. The SiPro MIPI IP solutions, used in a host of SoC mobile applications, are production-proven on the advanced 65nm LP process node and available on the 40nm LP process node.

Join the Virage Logic and Cadence MIPI Seminar

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Join Virage Logic and Cadence Design Systems Inc. on Wednesday April 21st at Cadence Design Systems, Inc. headquarters, 2655 Seely Avenue in San Jose, CA 95134 USA. Registration begins at 10:15am. The education seminar covers SoC design challenges for MIPI users and the agenda includes an introduction and latest developments to the MIPI standards, followed by a description of Virage Logic's production proven MIPI design IP and concluding with a presentation on Cadence Design's verification IP. Lunch will be served. [Click here to register for the event.](#)

Availability

All SiPro MIPI Rx and Tx D-PHYs and SiPro MIPI CSI Rx and DSI Tx controllers IP are available and shipping on the 65nm LP process. The SiPro MIPI Rx D-PHY and SiPro MIPI Tx D-PHY will be available Q2 2010 on the 40nm LP process.

About Virage Logic

Virage Logic is a leading provider of semiconductor intellectual property (IP) for the design of complex integrated circuits. The company's highly differentiated product portfolio includes processor solutions, interface IP solutions, embedded SRAMs and NVMs, embedded test and yield optimization solutions, logic libraries, and memory development software. As the industry's trusted semiconductor IP partner, more than 400 foundry, IDM and fabless customers rely on Virage Logic to achieve higher performance, lower power, higher density and optimal yield, as well as shorten time-to-market and time-to-volume. For further information, visit <http://www.viragelogic.com> [1].

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