# Universal PLD test system can perform boundary scan IC and board tests


Saelig Company has introduced the JTAGMaster Tester/Programmer, an integrated solution for testing and configuring Programmable Logic Devices (PLDs). JTAGMaster can perform boundary scan IC and board tests, as well as programming JTAG-compatible IC and EEPROMs using external adapters. JTAG is a standard IEEE1149.1 protocol which provides as access port to devices or printed circuit boards. What sets the JTAGMaster apart is its easy-to-use, configurable PC software.

SPI, I2C, and Microwire protocols are supported by the JTAGMaster, so it can program devices or PLDs in-system (Altera, Xilinx, Lattice, etc.) or program EEPROMs out-of-circuit via SPI, I2C, Microwire. It can program multiple boards at the same time, or write foolproof programming procedures. The JTAGMaster provides In-System Programming (ISP) via two standard headers conforming to Altera and Xilinx models, but a wide variety of other devices can be programmed using the configurable ISP interface cable provided. ISP sends programming, erasing, and other test instructions to ICs, even those assembled on printed circuit boards.

The JTAGMaster's software is a powerful, flexible, and customizable platform with application windows that can be redesigned by administrators to suit the particular needs or levels of operators. Visual appearance layouts can be rearranged and instructions, photos, or schematics can be added - including PDFs and web content. Access levels can be easily managed through user names and passwords. A key feature of the software allows system administrators to create automated step-by-

step programming sequences, with each step customized with photos, schematics, or instructions as simple or complex as required. Operators can be prompted to add comments at appropriate junctures, which are included in final reports.

Boundary-scan testing allows an operator to arbitrarily observe individual pins on a device and therefore determine correct functionality. The programming capability uses industry-standard JAM STAPL files (Standard test And Programming Language) and SVF (Serial Vector Format) files for programming as well as testing devices. The JTAGMaster is also capable of programming EEPROM devices using external adapters. Standard binary files are supported, which can also be modified in the device buffer window.

The JTAGMaster is aimed at the diagnosis and debugging of complex PCB assemblies containing single or multiple embedded devices, on static or active boards. It can detect manufacturing defects (open circuit/shorted pins), logic errors (pins not toggling/faulty device), program errors (incorrect/corrupted program) or faults in external circuitry (missing or stuck input signal), etc. With widespread application in electronics design and manufacturing, the JTAGMaster covers almost any JTAG programming need.

www.saelig.com [1]



**Links:**
[1] http://r20.rs6.net/tn.jsp?e=001wgpiSwXnbRSw5skz1QhqFOmwfzMkOn1Xy9fXMERKoPLwC8F-mHG-lvbjtVFSR0ZvUnoU-mqd_XrPzdygmXZTDCW5nSccTOjYaosm7w32zZY=