FPGA mezzanine card rapid prototyping kit aids JESD204B-compatible ADC-to-FPGA connectivity

Analog Device added to its line of FPGA development platform-compatible FPGA mezzanine cards (FMC) incorporating JEDEC JESD204B SerDes (serializer/de-serializer) technology. Digital and analog designers can use the AD9250-FMC-250EBZ kit to simplify and rapidly prototype high-speed JESD204B A/D converter-to-FPGA platforms. The AD9250-FMC-250EBZ features two AD9250 dual 14-bit high-speed JESD204B data converters providing four 14-bit A/D converter channels at 250 MSPS in an FMC-compliant form factor. The two on-board AD9250 A/D converters support Subclass 0 and 1 deterministic latency and provide a SYNCREF signal for precise synchronization of all four channels providing the connectivity and functionality to quickly combine with Xilinx’s Kintex-6/7 and Virtex-6/7 FPGA platforms in a variety of compute-intensive FPGA-based applications.

The AD9250-FMC-250EBZ FMC kit was designed with a multistage, differential pipelined architecture and integrated output error correction logic. The FMC may be clocked by either an internal clock source or externally. It has an external trigger input for customized sampling control, a high-pin-count connector, front panel I/O and can be used in a conduction-cooled environment. The FMC allows flexible control on sampling frequency, analog input gain, and over-range detection through serial communication buses. It is equipped with power supply and temperature monitoring and offers several power-down modes to switch off unused functions or protect the card from overheating.

Analog Devices, www.analog.com [1]

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