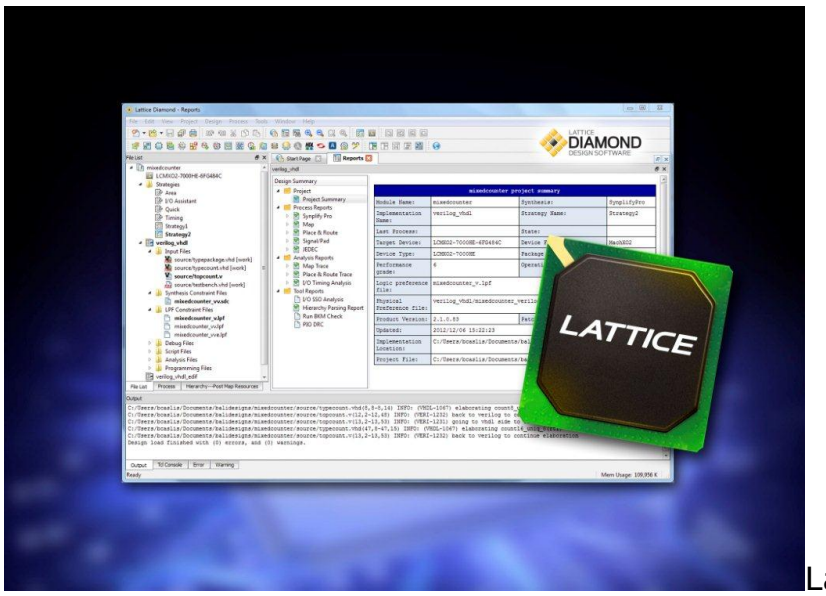
Software advancements allow for improved power calculations, design productivity



Lattice Semiconductor Corporation announced an array of advancements to its software platforms, debuting new versions of Lattice Diamond® and iCEcube2™ design tools. The updated software prominently features several notable advancements that improve power calculations and design productivity aimed at the creation of mobile and consumer, communication, and industrial systems that undergo fast design cycles, demand power efficiency, and have aggressive cost constraints.

Lattice Diamond 2.1

New Insights into Low Power Design
The updated Diamond Power Calculator contains a matrix that displays the power consumption of each block and each power supply. Also, the detailed power analysis for multiple design implementations can now be easily compared side by side in a new chart, extending the benefits of design exploration. For power- aware FPGAs such as the Lattice MachXO2™ device, designers, designers can view the detailed power analyses for the two power modes side by side.

Enhanced Design Exploration
Lattice Diamond software is designed to simply, create, and explore different design implementations to achieve the aggressive design goals of low cost, high volume designs. New algorithms further speed timing closure for multipass runs. By dynamically fine tuning the netlist during placement to meet the characteristics of the device, innovative algorithms for the LatticeECP3™ FPGA family achieve faster performance in the target device without incurring area penalties and increasing cost. Moreover, timing reports now include enhanced information on unconstrained

timing paths that accelerates the analysis of design constraints and timing results.

New Upgrades Boost Ease of Use
Lattice Diamond 2.1 software's Hierarchy view is now automatically available alongside the File List and Process views. It displays design resource usage at various stages of the implementation process, and allows the user to move directly to the HDL source for each level of hierarchy, to designate any level of the hierarchy as the top of the design, and to generate symbols for any level of hierarchy.

Verification and debug has also been upgraded. The Reveal™ debugger now supports debug insertion into a mixed language design at the HDL level, preserving buses and type information. The Simulation Wizard has new options that allow users unfamiliar with simulators to easily start simulations and trace signals.

To further help designers, updated documentation includes an expanded FPGA Design Guide with more information on HDL coding guidelines and timing analysis. A new tutorial provides in-depth information to help new users to begin working with the Lattice Diamond software.

The LatticeMico™ System's capability for generating system platforms has also been improved. Now, designers can easily expand the peripheral set of their microcontroller by connecting it to an FPGA that contains a peripheral-only platform generated by the LatticeMico System.

Ultra-Low Density FPGA Design Software for iCE40™
iCEcube2 software is the design environment for the Lattice iCE40 family of ultra-low density FPGA devices. The updated iCEcube2 software includes improvements that increase accuracy. For example, the new version of iCEcube2 software now includes final timing and power data that enable design analysis under worst case as well as typical conditions. The updated data also reflect wider temperature ranges to support both commercial and industrial devices, which gives designers greater confidence that their design will operate correctly in a variety of conditions. The power estimator also has improved data and algorithms that increase the accuracy of dynamic and static power calculations.

Lattice Semiconductor Corporation
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