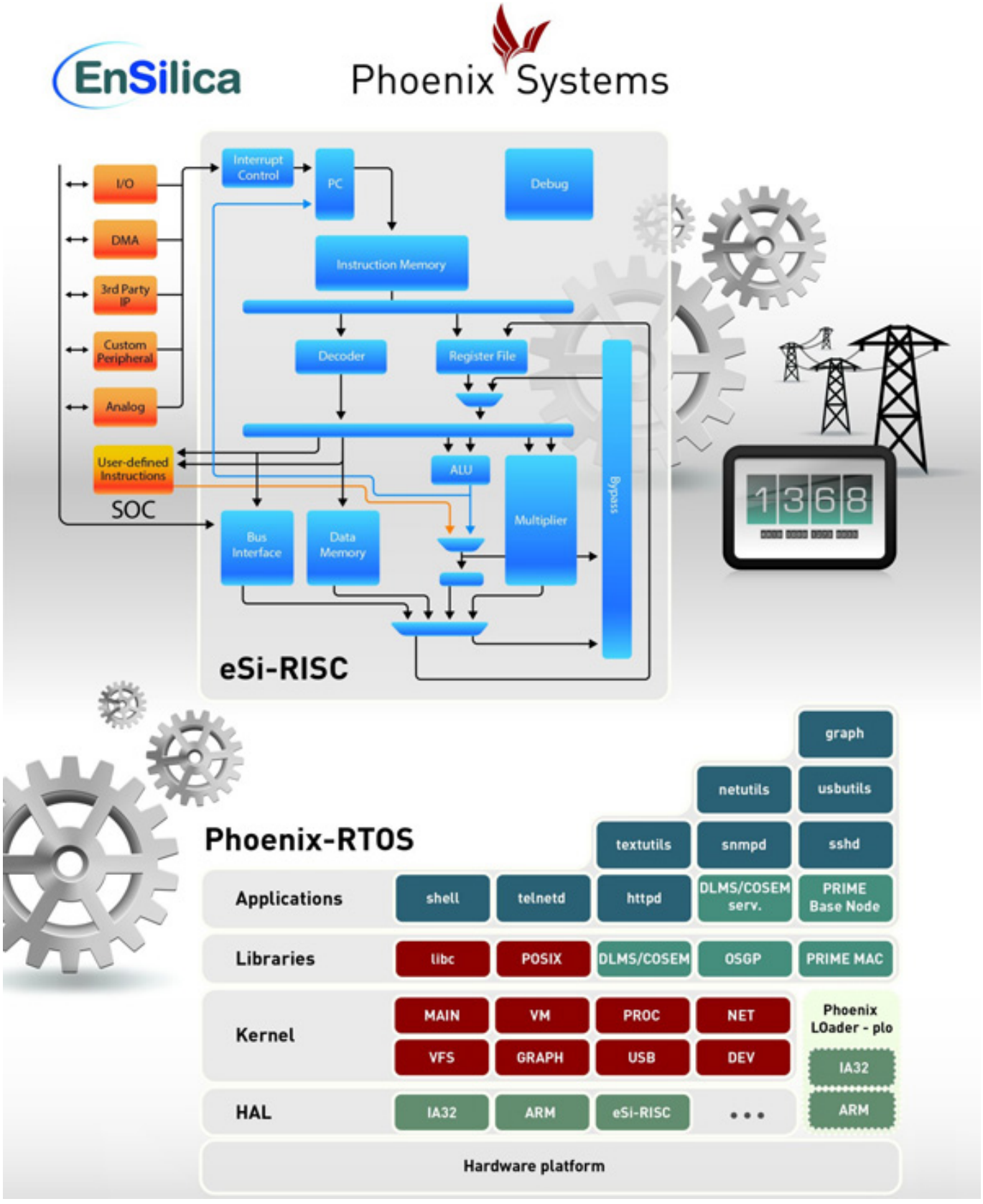
Processor family designed for both single and multicore embedded applications

EnSilica and Phoenix Systems have announced that they have successfully ported the Phoenix-RTOS, designed specifically for both single and multicore embedded systems applications, to the eSi-RISC family of highly configurable soft processor cores. The collaboration between EnSilica and Phoenix Systems further expands the eSi-RISC ecosystem with an embedded RTOS capable of fully utilising eSi-RISC’s hardware MMU with memory protection and security features such as data execution protection. It also paves the way for embedded power line and wireless smart grid solutions with the combination of Phoenix Systems’ proposed smart grid software protocol stacks and eSi-RISC’s support for custom instructions accelerating performance and improving PHY layer implementations.



Phoenix Systems' Phoenix-RTOS is a state-of-the-art, fully proprietary, real-time operating system designed specifically for both single and multicore embedded applications. Its modularity and portability, coupled with a small footprint, virtual memory support and an advanced architecture that implements the latest operating system mechanisms and programming abstractions, ideally suit it to use

with highly configurable soft processor cores like the eSi-RISC family. The fully re-entrant and pre-emptive kernel supports scheduling strategies that allow for the prioritization of critical task execution. Additional components, such as TCP/IP and USB stacks, common file systems and POSIX interface, further leverage its potential for machine-to-machine communication and smart grid applications.

EnSilica’s eSi-RISC family provides a range of high quality, highly configurable embedded processors that are easy to integrate. The processor subsystem is delivered fully targeted to customers’ ASIC technology, thereby reducing integration effort. eSi-RISC processors provide the flexibility to define a range of hardware functions to optimize the silicon area. On–chip memory requirements are reduced through inter-mixed 16-bit and 32-bit instructions, resulting in good code density without compromising performance. The incorporation of a hardware MMU coupled with multiple execution privilege levels enable critical applications to be run separately to ensure they don't interfere with one another. eSi-RISC is the only processor family scalable from 16-bits to 32-bits, starting from as low as 8.5k gates. It utilizes the industry standard GNU optimizing C/C++ compiler and Eclipse IDE for rapid software development, and supports efficient debugging on the target through a JTAG interface and hardware breakpoints. The development suite, which will include Phoenix-RTOS in the next release, is common to both 16-bit and 32-bit processors, protecting users’ software investment.

For further information about EnSilica, visit http://www.ensilica.com [1].

Links:
[1] http://www.ensilica.com/