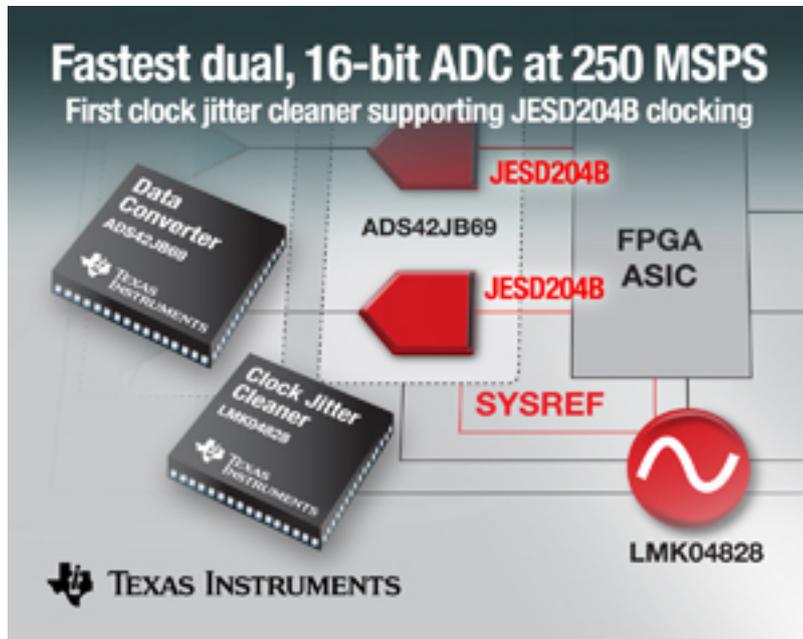


Dual, 16-bit ADCs for JESD204B market tout 250 MSPS speeds and clock jitter cleaner



Texas Instruments Incorporated

(TI) introduced a pair of devices supporting the JEDEC JESD204B serial interface standard for data converters. The ADS42JB69 is said to be the industry's first dual-channel, 16-bit analog-to-digital converter (ADC) featuring the JESD204B interface and is asserted to be the fastest at 250 MSPS. The LMK04828 is presented as the industry's highest-performance clock jitter cleaner and the first to support JESD204B clocking. When used together, the devices provide desirable system-level performance for high-speed systems. For designs requiring a traditional parallel interface, the company also introduced the ADS42LB69, a dual, 16-bit ADC at 250 MSPS featuring an LVDS interface. The ADS42JB69 incorporating all three JESD204B subclasses, 0, 1 and 2, allowing multi-device synchronization between data converters. The ADS42JB69 also supports the new JESD204B standard for deterministic latency, which provides fixed transmission delay with or without the use of an external timing signal. The device is also compatible with the existing JESD204A standard.

Features of the ADS42JB69 and ADS42LB69

- Highest dynamic performance to maximize receiver sensitivity: At 170 MHz intermediate frequency (IF), both ADCs provide spurious-free dynamic range (SFDR) performance of 89 dBc, up to 9-dB better than the competition, along with SFDR of 100 dBc, excluding harmonic distortion 2 (HD2) and HD3, signal-to-noise ratio (SNR) performance of up to 74.9 decibels relative to full scale (dBFS) and channel isolation of 100 dB.
- Maximum design flexibility with three digital interface choices:

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- ADS42JB69 with JESD204B interface reduces the required number of data interface lanes from 17 to five, slashing board space while reducing design complexity.
- ADS42LB69 supports traditional parallel interface designs via 17 lanes of double data rate (DDR) low-voltage differential signaling (LVDS) or 10 lanes of quad data rate LVDS.
- Easy analog input interface: High-impedance analog input buffer with programmable full-scale range simplifies input filter design and drive circuitry. This also increases performance uniformity and device-to-device repeatability across the analog input frequency range.
- Lowest power consumption: The ADS42JB69 consumes 775 mW/channel, while the ADS42LB69 uses only 740 mW/channel.
- Pin-compatible family for design flexibility: The new ADCs are part of a family that includes pin-compatible, high-performance 14-bit options. The dual, 14-bit, 250-MSPS ADS42JB49 (JESD204B) and ADS42LB49 (LVDS) provide SFDR performance of 89 dBc and SNR performance of up to 73.4 dBFS at 170 MHz IF.

Combining the 16-bit ADS42JB69 with the LMK04828 provides an elegant and simple way for system designers to achieve JESD204B serial interface compliance with reduced bill of materials (BOM), along with unsurpassed performance. The LMK04828 provides ultra-low-jitter and phase noise, while generating the JESD204B subclass 1 system timing reference signal (SYSREF) required for multi-device synchronization.

Texas Instruments

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[1] <http://www.ti.com>