

Low-Power DSP Architecture Framework Serves Wide Array of Advanced Wireless Standards

CEVA unveiled the CEVA-XC4000, a fully programmable low-power DSP architecture framework supporting the most demanding communication standards for cellular, Wi-Fi, DTV, white space, and more. Building upon its highly successful predecessors, the CEVA-XC4000 architecture sets a new milestone for power efficiency and utilizes an innovative instruction set to enable highly complex, software-based baseband processing which otherwise could only be accomplished with dedicated hardware. Illustrating this, the CEVA-XC4000 delivers a 5X performance improvement over the CEVA-XC323 DSP for LTE-A processing, while consuming 50% less power.

The CEVA-XC4000 architecture is offered in a series of six fully programmable DSP cores, offering modem developers a wide spectrum of performance capabilities while complying with the most stringent power constraints. By taking advantage of a unified development infrastructure composed of code-compatible cores, a set of optimized software libraries and a single tool chain, customers can significantly reduce software development costs while leveraging their software investment in future products.

"The CEVA-XC4000 redefines the concept of a 'universal communication architecture', enabling every conceivable advanced cellular, connectivity, DTV, white space and powerline communication standard to be efficiently supported by a single DSP architecture," said Gideon Wertheizer, CEO of CEVA. "Incorporating new power management techniques, we were able to dramatically reduce the power consumption for high-performance software-based processing, paving the way for modem developers to exploit the flexibility, reusability and time-to-market advantages that a software-defined approach brings."

"Today's advanced wireless communications landscape is a complex array of evolving standards and protocols that product developers must support quickly, cost-effectively and efficiently," noted Linley Gwennap, principal analyst of The Linley Group. "Based on the widespread adoption of its CEVA-XC architecture, the company has already delivered a programmable platform that meets the performance, power and die area requirements for today's baseband applications. CEVA's new XC4000 architecture is a scalable architecture with improved computational efficiency for next-generation wireless standards such as LTE-A and 802.11ac."

Power, Performance, Precision, System Know-how

Addressing the ever-increasing requirement for higher performance together with lower power consumption, the CEVA-XC4000 architecture incorporates new and innovative power-oriented enhancements, including CEVA's second generation Power Scaling Unit (PSU 2.0) which dynamically supports clock and voltage scaling

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with fine granularity within the processor, memories, buses and system resources. The architecture also utilizes Tightly Coupled Extensions (TCE) to deliver inter-connected power-optimized coprocessors and interfaces for the implementation of critical PHY functions, further reducing power consumption. A rebalanced pipeline with low-level module isolation is also highly optimized for power.

The CEVA-XC4000 incorporates enhanced system-level mechanisms, queues and interfaces to deliver exceptional performance, realizing faster connectivity, higher bandwidth, lower latency and better PHY control. The architecture offers uncompromising modem quality using two distinct inter-mixable high-precision instruction sets, supporting the most advanced 4x4 and 8x8 MIMO algorithms.

In order to better serve CEVA-XC4000 customers, CEVA has also announced today complete reference architectures targeting complex communication standards, including LTE-A Rel-10 and Wi-Fi 802.11ac supporting up to 1.7 Gbps, in collaboration with CEVA-XCnet partners mimoOn and Antcor. These reference architectures are complemented with highly optimized software libraries for LTE-A and Wi-Fi.

Streamlined Software Development

The CEVA-XC4000 DSP architecture is supported by CEVA-Toolbox, a complete software development environment, incorporating Vec-C™ compiler technology for advanced vector processors, enabling the entire architecture to be programmed in C-level. An integrated simulator provides accurate and efficient verification of the entire system including the memory sub-systems. In addition, CEVA-Toolbox includes libraries, a graphical debugger, and a complete optimization tool chain named CEVA Application Optimizer. The Application Optimizer enables automatic and manual optimization applied in the C source code.

For more information, visit www.ceva-dsp.com/CEVA-XC4000.html [1]

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