Improved Test Bench Generation for Multi-Chip Modules and 3D Chips

GOEPEL electronic announces the availability of additional features in its EDA software TAPChecker for the generation of BSDL test benches. The newly developed options extend the software's flexibility in terms of handling pin groups and complex port declarations for improved coverage of multi-chip modules and 3D chips. Users are now able to assign special vector sequences to complete port groups or to adopt complex bus structures into the simulation. All new options are customer driven.

"The success of TAPChecker with leading semiconductor manufacturers in Asia, Europe and the USA not only proves our software's quality. It is especially commitment to our customers to provide features, necessary for their chip development, functionally and on time," says Thomas Wenzel, Managing Director of GOEPEL electronic's JTAG/Boundary Scan Division. "With our tools we keep up with the rapid development in integration technologies for multi-chip modules and 3D chips".

TAP Checker is based on modular platform architecture with a central database and individual licensed modules for data import/export and automatic test vector generation. The software was designed for automatic test bench generation for simulations based on BSDL files as well as provision of test vectors for In-Circuit Testers. It can be utilised in various operating systems such as SOLARIS, Windows and LINUX, supporting the Boundary Scan standards IEEE 1149.1 and IEEE 1149.6.

The new features are available from TAPChecker V. 2.2 on. The release is already shipping, free-of-charge for users with valid maintenance contract. Die Auslieferung des Release hat bereits begonnen und ist für Anwender mit gültigem Wartungsvertrag kostenlos.

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