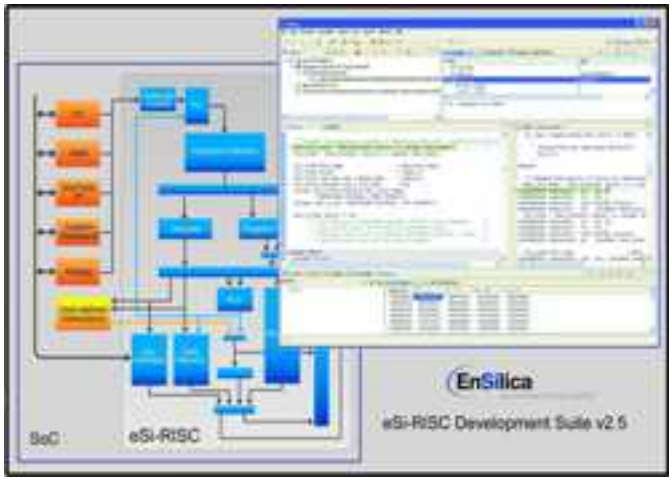
EnSilica launches Updated eSi-RISC Development Suite



EnSilica, a leading independent provider of IC design services and system solutions, has launched the eSi-RISC Development Suite v2.5, a major new version of its complete development environment for evaluating the EnSilica family of eSi-RISC highly configurable and low-power soft processor cores and the development of embedded applications. The eSi-RISC Development Suite v2.5 features new capabilities for multicore support, significantly enhanced compiler performance and ultra low-power applications support.

With the increasing trend towards multicore eSi-RISC designs such as dual core secure processor applications and Posedge’s innovative 7-core Residential and SMB Gateway, the eSi-RISC development Suite v2.5 now provides JTAG debug and control over all processors in the JTAG chain. In addition, optional load locked and store conditional instructions have been added to the instruction set to support multicore systems.

Compiler performance has also been enhanced with the provision of Link Time Optimization (LTO) support which can improve code density by between 10% and 15% through expanding the scope of inter-procedural optimizations to encompass the whole program. This has been achieved by upgrading the optimizing C/C++ compiler to GNU GCC version 4.6.1. Additionally, benchmarking the eSi-3250 32-bit processor core using the embedded processor CoreMark benchmark, which is rapidly replacing the traditional Dhrystone MIPS benchmark, shows it performs exceptionally well, delivering 2.359 CoreMark/MHz.

An approximate power reduction of 15% has been achieved with the inclusion of improved clock gating and operand isolation optimization in the RTL. This makes the eSi-1600 16-bit processor core an extremely viable ultra low-power alternative to 32-bit CPU or legacy 8-bit architectures (such as the 8051) and ideally suited for mixed signal applications.

The eSi-RISC Development Suite v2.5 also incorporates new peripherals including an AMBA AHB compatible static memory interface for external Flash and SRAM memory, AMBA AHB DMA Engine, AMBA APB I2C Slave and AMBA APB Smart Card interface supporting ISO-7816 standard. These have been added to the current eSi-Connect portfolio which already includes SPI, UART USB, I2C Master, Ethernet MAC, RTC and Timer peripherals.

Finally, support for Linux is also now provided with the latest port of the GCC, GDB Debugger and GNU binary tools. Additional software examples and documentation have also been included to speed up evaluation and development. New application examples include a port of FreeRTOS, LwIP TCP/IP Stack and web server as well as SPI Memory and CFI Flash programmer.

“The ease and speed with which processors can be evaluated and applications developed and tested, plays an important role in developers’ choice of processors,” said Ian Lankshear, CEO of EnSilica. “The eSi-RISC Development Suite v2.5 includes a host of new features and capabilities to enable our eSi-RISC processor family to be easily evaluated and quickly deployed.”

About EnSilica’s eSi-RISC family

EnSilica’s eSi-RISC family provides a range of high quality, highly configurable embedded processors that are easy to integrate. The processor subsystem is delivered fully targeted to customers’ ASIC technology, thereby reducing the integration effort. eSi-RISC processors provide the flexibility to define a range of hardware functions to optimize the silicon area. On–chip memory requirements are reduced through inter-mixed 16-bit and 32-bit instructions, resulting in good code density without compromising performance. It is the only processor scalable from 16-bits to 32-bits, starting from as low as 8.5k gates. eSi-RISC utilizes the industry standard GNU optimizing C/C++ compiler and Eclipse IDE for rapid software development, and supports efficient debugging on the target through a JTAG interface and hardware breakpoints. The development suite is common to both 16-bit and 32-bit processors, protecting users’ software investment.

For further information about EnSilica, visit http://www.ensilica.com [1].

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