FPGA embedded series enables flash programming

GOEPEL electronic announces the development of special ChipVORX model library series for FPGA accelerated in-system programming (ISP) of Flash components. The ChipVORX models developed in cooperation with the Tallinn/Estland based Company Testonica are structured modularly as intelligent IP. They enable the ultra fast in-system programming of every kind of Flash components at full workflow automation.

“The FPGA based accelerated procedure developed by Testonica enables the extremely fast Flash programming. Additionally it is fully automatable, which fits perfectly to our revolutionary new ChipVORX technology to control chip embedded instrumentations”, says Thomas Wenzel, GOEPEL electronic’s managing director of the Boundary Scan Division. By the complete integration into our SYSTEM CASCON software platform users can now fast and effectively program massive Flash images with the existing tool suite. Furthermore, the tremendous advantages in in-system programming can be implemented even stronger in particular in the production process and will replace cost intensive stand-alone solutions.”

Dr. Artur Jutman, Testonica Lab's Director adds: “Our key challenge was to deliver customers a technology with a great added value and absolutely no penalty in form of personnel training and extra time spent for project configuration. Now, engineers can considerably speed-up their in-system programming tasks just by enabling a license. The technology will be demanded in applications involving large flash memories especially flash ICs equipped with a serial interface.”

Due to the complete integration of the ChipVORX IP the recognition of the structural connections between Flash target and FPGA is done as automatically as the succeeding script file generation. The programming is based on a standardised IEEE1149.1 TAP (Test Access Port) and can be executed on each run time station without further options. Thereby, Gang applications are supported.

Because of the ChipVORX IP’s independence of the target to be programmed the Flash type imposes no restrictions. In addition to serial Flash, parallel NOR and NAND Flash incl. bad block handling is supported. As the same system libraries as for a “normal” Boundary Scan programming are used, users may update new Flash models by themselves.

In practice, the ChipVORX IP’s achieves drastic accelerations for bigger FPGA types compared to standard Boundary Scan programming procedures. Whilst typical values for parallel Flash are between 10 and 15 times, the factor for serial Flash achieves a size of 100 times and even higher. The acceleration is only limited by the Flash internal programming speed.

At the moment, the ChipVORX models for Flash programming are available for all Altera and Xilinx FPGA families, additional ones are under development. The usage of the IP does neither require expert background knowledge nor special FPGA tools or programmers. Due to the OEM cooperation with all leading vendors of In-Circuit Testers (ICT), Manufacturing Defect Analysers (MDA), Flying Probe Testers (FPT) and Functionality Testers (FT), the new solution is available for production with immediate effect.

The new ChipVORX IP models are supported as standard starting from SYSTEM CASCON version 4.5.4 and are activated by the licence manager like the system software. SYSTEM CASCON is a professional JTAG/Boundary Scan development environment, developed by GOEPEL electronic with currently 45 completely integrated ISP, test, and debug tools. Regarding the hardware, VarioTAP is completely supported by the controllers of the SCANBOOSTER family, as well as by the hardware platform SCANFLEX.

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