Evatronix Releases USB 2.0 High Speed PHY to Complement its USB Offering

Evatronix SA, announced today the introduction of a USB High Speed PHY IP that will complement the long-existing suite of USB 2.0 Device and Host controllers. Evatronix USB 2.0 PHY has already been silicon proven and guarantees compliance with all relevant layers of USB specification for High, Full and Low Speeds.

“With the release of our USB 2.0 PHY we passed next significant milestone in our strategy to offer complete front-to-back IP solutions,” said Wojciech Sakowski, Evatronix CEO. “With over 10 years of experience in developing and supporting USB 2.0 solutions we can now seamlessly assist our customers in all their development stages from architectural concept to tape-out.”

The Evatronix USBHS-PHY is a complete mixed-signal transceiver macro-cell that implements the USB 2.0 Physical Layer for Host and Device applications. It is compliant with the UTMI+ specification.

The Evatronix USBHS-PHY features a Built-in Self Test, self calibration termination and pull-up resistors for seamless operation. It also supports regular 3.3V analog and 1.8V digital core supplies, both with 10% of voltage tolerance. Numerous other features enable designers to tailor the USBHS-PHY to the needs of a particular application.

EVATRONIX USBHS-PHY AVAILABILITY
The Evatronix USBHS-PHY logic macro is available now on the LFoundry 150nm process with the possibility to port it to any technology node from 45 to 180nm.

For more information please visit the company’s web site at www.evatronix.com/ip [1]

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