C-to-FPGA Compiler Accelerates Image Processing

Impulse Accelerated Technologies today announced version 3.7 of its CoDeveloper C-to-FPGA Optimizing Compiler. CoDeveloper, used worldwide by nearly 500 customers, is a C-language development environment for FPGAs that allows software algorithms to be quickly and efficiently implemented in programmable hardware. This CoDeveloper update includes improvements to compiler performance, expanded Linux support and new parallel hardware optimization features including support for higher-throughput streaming I/O.

CoDeveloper 3.7 improvements include timing optimizations that speed up generated pipelines by optimizing out unnecessary dependencies in address generation, and other optimizations that identify and improve state-enable dependencies for more efficient parallel statement scheduling. For selected platform targets, local FPGA memory can now be banked, allowing streaming reads and writes to access memories at a wider width than the actual array element width. To cite one example, an array of bytes can be generated with eight banks allowing stream reads and writes to process 64 bits per cycle, effectively increasing host I/O by 8X or even 16X.

CoDeveloper 3.7 also brings the Linux version much closer to the Windows version by providing graphical capabilities for the Stage Master Explorer and Debugger tools. For pipeline and parallel statement analysis, dataflow graphs are now created dynamically in the Stage Master Explorer tool for improved responsiveness, and panning and zooming features have been improved for exploring very large and wide pipeline structures. Also, functions can now be debugged by clicking on the function call to open new window displaying the function state.

CoDeveloper 3.7 focuses on quality of results (QOR) in the compiler, and in particular on features that assist with pipeline optimization and streaming I/O performance. “A key metric of software-to-hardware compilers is QOR relative to design effort,” said David Buechner, Impulse VP of Business Development. “Impulse users have reported that they create, test and iterate QOR improvements 80% faster using Impulse C than when using a traditional HDL design method. And when needed, Impulse C users can integrate previously optimized HDL into their C-language applications.”

For FPGA design engineers, QOR is often characterized by how small and efficient a given block of code will compile down to bitmaps running on the FPGA, and the clock speeds achievable in the resulting hardware. However, for many higher-level applications, the ability to control the hardware generation process during algorithm refactoring can result in even greater gains in performance, especially for C algorithms that are being re-implemented using streaming, pipelining, and multiple-process parallelism.

“C is making inroads into FPGA design,” said Brian Durwood, Impulse CEO. “Or rather, FPGAs are making inroads into processing domains that previously would have been owned by microprocessors, DSPs or high performance servers. Such domains where we are seeing strong growth in C-to-FPGA usage include bioinformatics, video processing, defense, and financial computing, particularly high-frequency trading. A key factor in all of these domains has been the availability of higher level, more software-like tools, and the ability for software/hardware groups to work together while speaking a common language – in this case C.”

CoDeveloper 3.7 update is available free of charge to licensed users of the CoDeveloper software who have active maintenance agreements.