Data Converters Reduce Board Space In High-Speed Applications

Analog Devices, Inc. (ADI) announced today a pair of low-power, high-speed 14-bit ADCs (analog-to-digital converters) that incorporate the JESD204A data converter serial interface standard. The JESD204A standard was developed to allow designers of high-speed communications and data acquisition systems to extend transmission lengths while improving signal integrity and simplifying printed-circuit board layout. The AD9644 dual and AD9641 14-bit 80 MSPS (mega samples per second) ADCs use half the power of competing products and 25 percent less board area further expanding ADI’s portfolio of high-speed ADCs supporting the JESD204A standard.

The JESD204A industry serial interface standard reduces the number of data inputs/outputs between data converters and other devices, such as FPGAs (field-programmable gate arrays). Fewer interconnects simplifies layout and allows smaller form factor realization without impacting overall system performance. These attributes are important for a range of high-speed applications, including portable instrumentation, ultrasound equipment, radar, wireless infrastructure (GSM, EDGE, W-CDMA, LTE, CDMA2000, WiMAX, TD-SCDMA), and software-defined radios. For more information about the AD9644 dual 14-bit ADC, go to http://www.analog.com/pr/AD9644 or to learn more about the AD9641 ADC, go to http://www.analog.com/pr/AD9641 [1].

About the AD9644 Dual 14-bit 80MSPS with JEDS204A Interface

The AD9644 consumes 423 mW at 80 MSPS and features a multi-stage, differential-pipelined architecture with integrated output error correction logic. At 70 MHz and 80 MSPS, the AD9644 achieves an SNR (signal-to-noise ratio) of 73.7 dBFS and an

SFDR (spurious-free dynamic range) of 92 dBc. The JESD204A coded data rate supports up to 1.6 Gbps per link and the AD9644 offers two output modes supporting a dedicated data link per ADC channel or a single shared data link for both ADC channels. Wide bandwidth differential sample-and-hold analog input amplifiers support a variety of user-selectable input ranges while an integrated voltage reference eases design considerations. A duty cycle stabilizer is provided to compensate for variations in the ADC clock duty cycle, allowing the converters to maintain excellent performance. The AD9644 is available in a 48-lead LFCSP (7 mm x 7 mm) and is specified over the industrial temperature range of -40°C to +85°C.

AD9644 Dual 14-bit ADC Key Features

• 80 MSPS Sample Rates
• 14-Bit Resolution
• Two configurable serial outputs
• SNR: 73.7 dBFS at 70 MHz and 80 MSPS
• SFDR: 92 dBc at 70 MHz and 80 MSPS
• Low power: 212 mW/channel at 80 MSPS
• Single 1.8-V supply operation

As part of a complete signal chain, the AD9644 and AD9641 can be used with amplifiers, VGAs and clock drivers such as the ADL5562 3.3 GHz ultralow -distortion RF/IF differential amplifier, ADA4937-2 ultralow -distortion differential ADC driver, AD8372 programmable dual VGA, AD9510 clock distribution IC and AD9520 CMOS output clock generator with integrated VCO.

More Information, Samples and Tools

• For more information: http://www.analog.com/pr/AD9644 or http://www.analog.com/pr/AD9641 [1]
• Visit the AD9644 data sheet
• For data converter design tools: http://www.analog.com/ADC-Tools [2]
• For more data converter information: visit http://www.analog.com/Data-Converters [3]

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Links:
[1] http://www.analog.com/pr/AD9641
[2] http://www.analog.com/ADC-Tools
[3] http://www.analog.com/Data-Converters