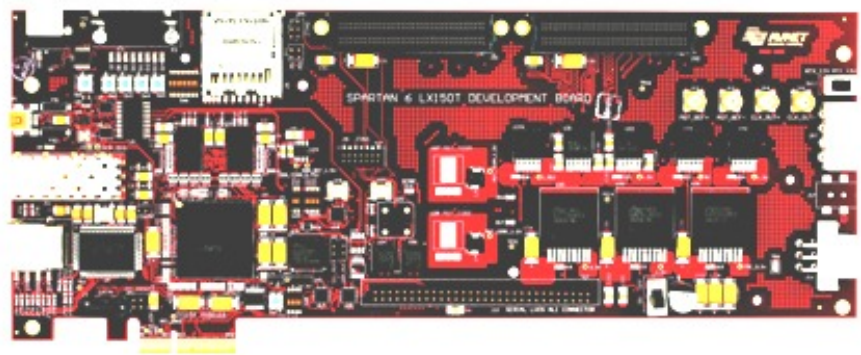
Development Kit Jump Starts DSP Designs



The Spartan-6 FPGA DSP Development Kit from Avnet enables users to focus on the unique value of their design with an easy entry point for using FPGAs for DSP. Aerospace and defense, wireless, ISM and other computationally-intensive applications demand digital signal processing performance and cost effective solutions. “With the introduction of the Spartan-6 FPGA DSP Kit, Avnet is offering its first DSP development platform for customers who need greater performance and low cost,” said Jim Beneke, vice president, global technical marketing at Avnet Electronics Marketing. “This kit will help our customers quickly learn the different tool flows and design techniques involved in creating DSP-centric designs with the Spartan-6 FPGA family.”

The Spartan-6 FPGA DSP Development Kit combines a scalable development board, DSP IP, DSP Development tools, and a preconfigured and fully validated Spartan-6 DSP Targeted Reference Design. This design serves as a basis to illustrate DSP techniques and design flows for the Spartan-6 class of signal processing functions. The state of the art digital up converter (DUC) / digital down converter (DDC) Targeted Reference Design shows customers how to use advanced techniques such as clock over-sampling, time division multiplexing and signal processing and resource optimization with the high performance DSP48 slices. Both an RTL and Model-Based Design flows are included. The design flow, based on MATLAB® and Simulink® from the MathWorks™, allows algorithm developers to create DSP hardware designs using a familiar modeling environment without the need to learn RTL. Experienced RTL designers are provided design techniques for creating efficient DSP hardware using ISE Design Suite and LogicCore™ DSP IP along with verification methodologies for comparing functional correctness against high-level algorithm models.

Key deliverables of the Spartan-6 DSP Targeted Reference Design are:

- Design source files for RTL and Simulink
- Top level system integration RTL source files
- Simulation environment
- Testbenches

- Implementation environment
- Complete steps and parameters for design synthesis
- MAP, place and route and timing closure
- Targeted reference design tutorials including recommended flows for design modification and integration

“MathWorks is very pleased to have design flows using MATLAB and Simulink included as part of the Xilinx Spartan-6 FPGA Kit,” says Amnon Gai, manager in MathWorks corporate development and partner programs group. “Model-Based Design using Simulink eases the adoption of FPGAs and significantly accelerates FPGA implementation of signal processing, computer vision and control system applications. With Xilinx System Generator it provides a turnkey rapid prototyping solution for engineers new to FPGAs without RTL design experience.”

Order entry is now open for the $1,995 kit, which includes a device-locked version of ISE Design Suite: System Edition 11.4. For complete kit specs and to purchase, please visit http://em.avnet.com/spartan6dsp [1].

Links:
[1] http://em.avnet.com/spartan6dsp