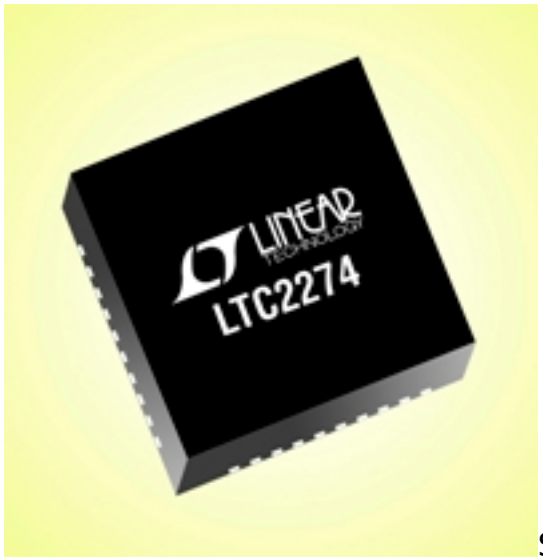
ADC Saves I/O Lines in FPGAs



Streamlining the digital communication between high speed ADCs and FPGAs, the Linear Technology LTC2274 16-bit, 105Msps ADC reduces the number of data I/O lines required between the ADC and the FPGA from 16 CMOS or 32 LVDS parallel data lines to a single, self-clocking, differential pair communicating at 2.1Gbps. Consuming 1.3W from a 3.3V analog supply, the 6mm² QFN-40-packaged device includes features such as a signal-to-noise ratio of 77.5dB, an SFDR of 100dB at baseband, and a jitter of 80fs RMS for undersampling of input frequencies up to 500MHz. The ADC's output is serialized according to JESD204 using 8b10b encoding, and is compatible with many FPGA interfaces including Xilinx's Rocket, Altera's Stratix II GX, and Lattice's ECP2M. From $68.00 each in 1,000-piece quantities.

Linear Technology
408-432-1900, www.linear.com [1]

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