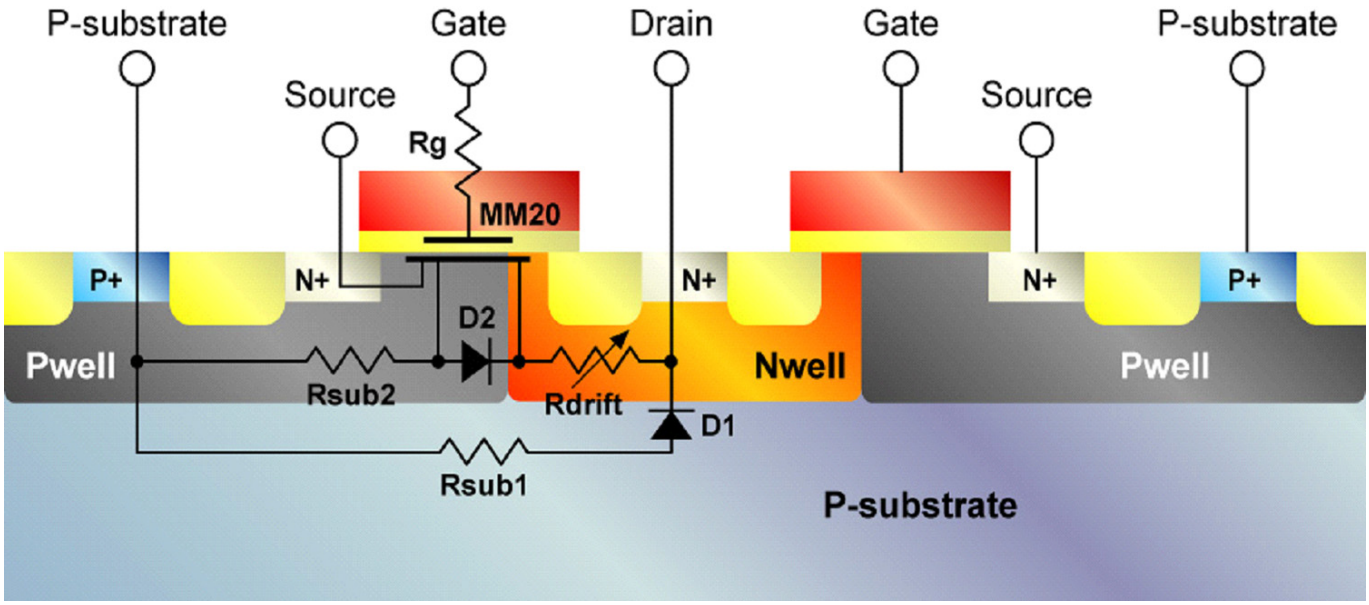
BCD Process Enables 50 Percent Power Die Size Reduction

Jazz Semiconductor has developed enhancements to its advanced Bipolar CMOS DMOS (BCD) process platform including the addition of an ultra low $R_{ds(on)}$ scalable NLDMOS device enables up to a 50 percent shrink in die size in most power devices. The 0.18 µm BCD process adds the combination of high density 1.8-V digital CMOS with the higher voltage drivers required for highly integrated Power SOC designs. The high-voltage BCD process is available in scales from 0.5µ to 0.18µ with features includeing VIA stacking, thick top power metal (3 µm) for improved current-carrying capacity, ESD protection circuits, and triple well isolation.



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