

## **The Tinker's Toolbox - Marc Serughetti of Synopsys on Virtual Prototyping**



Hosted by Alix Paultre, the Tinker's Toolbox is the Advantage Design Group's web-based interview show where we talk about the latest technology, components, and design issues for the electronic design engineering community.



In this podcast we talk to Marc Serughetti of Synopsys about next-generation virtual prototyping, systems simulation, and design. Synopsys is a world leader in electronic design automation, providing software, intellectual property, and services for semiconductor design, verification and manufacturing. Their integrated portfolio of implementation, verification, IP, manufacturing and FPGA solutions helps address key challenges such as power and yield management, system-to-silicon verification, and time-to-results.

[Right-click to download the podcast](#) [1]

Here is a link to the podcast in case the play button is inoperative: [Synopsys Call](#) [1]

Here is a presentation on their virtual prototyping technology: [Synopsys Presentation](#) [2]

Here is a recent release from the company:

Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP used in the design, verification and manufacture of electronic components and systems, today

announced updates to its [Identify](#) [3] and [Certify](#) [4] FPGA-based prototyping tools. Algorithm advancements in the latest Certify software release produce up to 30 percent faster FPGA-to-FPGA transmission performance using High-Speed Time Domain Multiplexing (HSTDM), which results in higher overall performance of designs prototyped with Synopsys' [HAPS](#) [5] FPGA-based prototyping systems. The new Certify and Identify software tools also incorporate incremental compilation technology that accelerates implementation of design revisions, as well as automation to ease the partitioning of large designs into multiple HAPS boards.

"The new Certify and Identify releases offer significant productivity gains and faster performance for ASIC prototyping engineers," said Wouter Suverkropp, product line marketing manager of Virtex-6 FPGAs at Xilinx, Inc. "When used with Synopsys' HAPS-60 series systems that can support up to 81 million ASIC gates, these releases are well suited to make the most of the powerful Virtex-6 LX760 devices that each provide 760,000 logic cell capacity, 26Mbits of internal memory, and 864 DSP blocks."

## **Certify Multi-FPGA ASIC Prototyping Software Delivers Higher Performance**

The latest release of the Certify multi-FPGA ASIC prototyping software incorporates new and enhanced features for higher prototype performance and greater ease of use with Synopsys' HAPS systems, allowing designers to:

- Increase the data throughput of prototypes enabled by up to 30 percent faster HSTDM of I/Os
- Quickly bring-up prototypes built with multiple HAPS boards using system target Tcl scripting
- Produce very accurate static timing analysis estimates with post-route delay back annotation
- Speed ASIC design migration with support for encrypted DesignWare® Library IP
- Obtain a more complete resource analysis of multi-FPGA designs with new PCB trace impact analysis

## **Identify RTL Debugger Enhances Visibility and Turnaround Time**

A high degree of visibility inside the FPGAs of the prototyping system significantly improves debugging efficiency. The latest release of Identify RTL debugger includes new and enhanced capabilities that improve debug throughout the design cycle and reduce turnaround time, allowing designers to:

- Understand prototype operation faster with debugger results annotated in the RTL View of the Synplify® HDL Analyst® graphical analysis tool
- Isolate defects by tracing longer periods of signal activity with up to 64

- times more sample buffer capacity
- Update and implement design instrumentation faster with Synplify compile point technology by preserving design modules not affected by debug instrumentation

Both software tools are designed for use with Synopsys' HAPS systems, though enhancements in these latest tool releases also benefit custom and build-your-own prototypers.

"As design complexity grows, it is increasingly important for developers to prototype their designs quickly and debug them efficiently," says Ed Bard, senior director of product marketing at Synopsys. "The new Identify and Certify tool releases include significant advancements in the FPGA software tool flow that directly translate to higher productivity for our HAPS users, and also ensure that designers who build their own hardware prototypes can do so faster and with less effort."

## Availability

Both of the latest tool releases for the [Certify](#) [4] multi-FPGA ASIC prototyping software and [Identify](#) [3] RTL Debugger are available immediately. For more information about the Certify tool, see the [datasheet](#) [6]. For more information about the Identify tool, see the [datasheet](#) [7].

## Source URL (retrieved on 12/09/2013 - 9:46pm):

[http://www.ecnmag.com/podcasts/2011/12/tinkers-toolbox-marc-serughetti-synopsys-virtual-prototyping?qt-recent\\_content=0](http://www.ecnmag.com/podcasts/2011/12/tinkers-toolbox-marc-serughetti-synopsys-virtual-prototyping?qt-recent_content=0)

## Links:

[1] <http://www.ecnmag.com/sites/ecnmag.com/files/legacyfiles/ECN/Multimedia/Audio/2011/12/synopsys.MP3>

[2] <http://www.ecnmag.com/sites/ecnmag.com/files/legacyfiles/ECN/Multimedia/Audio/2011/12/ReleasePresentation.pdf>

[3] <http://www.synopsys.com/Tools/Implementation/FPGAImplementation/FPGASynthesis/Pages/Identify.aspx>

[4] <http://www.synopsys.com/Systems/FPGABasedPrototyping/Pages/Certify.aspx>

[5] <http://www.synopsys.com/Systems/FPGABasedPrototyping/Pages/HAPS.aspx>

[6] <http://www.synopsys.com/cgi-bin/sld/pdfdla/pdfr1.cgi?file=certify-ds.pdf>

[7] [http://www.synopsys.com/Tools/Implementation/FPGAImplementation/CapsuleModule/identify\\_ds.pdf](http://www.synopsys.com/Tools/Implementation/FPGAImplementation/CapsuleModule/identify_ds.pdf)