The Tinker's Toolbox - Integrated CAN Transceiver Microcontroller Solution

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Hosted by ECN's Editorial Director, Alix Paultre, the Tinker's Toolbox is ECN's web-based interview show where we talk about the latest technology, components, and design issues for the electronic [1] design engineering community.

In this episode of the Tinker's Toolbox, we talk to Geoff Lees from NXP about their latest device, presented as the industry’s first integrated high-speed CAN Physical Layer transceiver and microcontroller with on-chip CANopen drivers.

Right-click to download the podcast [2]

Here is another link to the recording: NXP Interview [2]

Click here to view the NXP Presentation [3] on the device.

Here is the text of the product release:

NXP Semiconductors announced the LPC11C22 and LPC11C24 – the industry's first integrated high-speed CAN Physical Layer transceiver and microcontroller with easy-to-use on-chip CANopen drivers. Offered as a unique System-in-Package solution, the LPC11C22 and LPC11C24 with integrated TJF1051 CAN transceiver combine complete CAN functionality into a low-cost LQFP48 package.

CAN is recognized as a robust and reliable communication channel for rugged environments. With the introduction of the LPC11C22 and LPC11C24 integrated CAN transceiver microcontroller solution, NXP has opened the door for widespread adoption of low-cost CAN in an increasing variety of industrial and automation applications for factories, buildings and in the home. Typically, CAN transceivers can cost as much as or even more than the microcontroller itself. Integrating the CAN transceiver on board increases system reliability and quality, reduces electrical interconnect and compatibility issues, and reduces board space by over 50 percent while adding less than 20 percent to the MCU cost. The LPC11C22 and LPC11C24 are the latest additions to the LPC11C00 series of CAN 2.0B-compliant controllers.

"Offering a highly optimized CAN solution in a single package simplifies industrial network design," said Geoff Lees, vice president and general manager, microcontroller product line, NXP Semiconductors. "The close coupling of transceiver and 32-bit MCU with CANopen protocol support directly on-chip extends our plug-and-play system approach."

The CAN Physical Layer is designed for up to 1 Mbit/s High-Speed CAN networks and delivers optimal performance for industrial applications with state-of-the-art Electrostatic Discharge (ESD) protection, improved Electromagnetic Compatibility (EMC) and low power operation. The LPC11C22/C24 CAN Physical Layer is fully compliant with the ISO 11898-2 standard for two-wire balanced signaling and is optimized for automotive sensor applications and rugged industrial CAN networks. High ESD handling capability on bus pins is combined with additional fail-safe features such as high DC handling capability on CAN pins, Transmit Data dominant time-out function, undervoltage detection, and thermal protection. Low power management is fully integrated, and the transceiver can disengage from the bus when it is not powered up.

CANopen drivers are provided in on-chip ROM with easy-to-use APIs enabling users to rapidly adopt the LPC11C22/C24 into embedded networking applications based on the CANopen standard. This standardized CANopen layer (EN 50325) is especially well suited for embedded networks in all kinds of control, such as machines and elevators, making proprietary or application-specific application

layers obsolete. Incorporating CANopen drivers in on-chip ROM reduces overall risk and effort while providing design engineers with the added advantage of reduced operating power, as well as secure and safe bootloading via CAN. With the security and peace of mind offered by ROM-based drivers, updating Flash via In System Programming (ISP) over the CAN-bus provides the whole range of functionality – from programming blank parts in production, through changing system parameters, to full in-field re-programmability. The following functions are included in the API:

• CAN set-up and initialization
• CAN send and receive messages
• CAN status
• CANopen Object Dictionary
• CANopen SDO expedited communication
• CANopen SDO segmented communication primitives
• CANopen SDO fall-back handler

Enabling Higher Code Density and Superior Performance
The LPC11C22 and C24 require 40-50 percent smaller code size than 8/16 bit microcontrollers for most common microcontroller tasks. This is enabled by the powerful ARM® Cortex™-M0 v6-M instruction set, which is built on a fundamental base of 16-bit Thumb instructions unique to 32-bit microcontrollers today.

With over 45 DMIPS of performance, the LPC11C22 and LPC11C24 provide powerful message and data handling for CAN device nodes together with a power-optimized solution unavailable with today's 8-/16-bit microcontrollers.

Key features of the LPC11C22 and LPC11C24 include:

• 50 MHz Cortex-M0 processor with SWD/debug (4 break-points)
• 32KB/16KB Flash, 8KB SRAM
• 32 Vectored Interrupts; 4 priority levels; Dedicated Interrupts on up to 13 GPIOs
• CAN 2.0 B C_CAN controller with on-chip CANopen drivers, integrated transceiver
• UART, 2 SPI & I2C (FM+)
• Two 16-bit and 2 32-bit timers with PWM/Match/Capture and one 24-bit system timer
• 12MHz Internal RC Oscillator with 1% accuracy over temperature and voltage
• Power-On-Reset (POR); Multi-level Brown-Out-Detect (BOD); 10-50 MHz Phase-Locked Loop (PLL)
• 8-channel high precision 10-bit ADC with ±1LSB DNL
• 36 fast 5V tolerant GPIO pins, high drive (20 mA) on select pins
• High ESD performance: 8kV (Transceiver) / 6.5kV (Microcontroller)
• Low Electromagnetic Emission (EME) and high Electromagnetic Immunity (EMI) CAN transceiver

For further information on the LPC11C00 series, please visit:
http://ics.nxp.com/products/lpc1000/lpc11xx/lpc11cxx/ [4].
For further information on all NXP Cortex-M0 families, please visit:
http://www.nxp.com/cortex-m0 [5].

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