Chandrakasan selected for 2013 IEEE Pederson Award in Solid-State Circuits

Massachusetts Institute of Technology
Anantha P. Chandrakasan — the Joseph F. and Nancy P. Keithley Professor of Electrical Engineering at MIT and head of the Department of Electrical Engineering and Computer Science (EECS) — is the 2013 recipient of the IEEE Donald O. Pederson Award in Solid-State Circuits [1]. He was cited in the award for "pioneering techniques in low-power digital and analog CMOS design."

The Solid-State Circuits Award, inaugurated in 1987, is the most prestigious IEEE award in the field of semiconductor circuits. The award was renamed in 2005 to honor Professor Donald O. Pederson, who was instrumental in establishing the IEEE Solid-State Circuits Society and the *IEEE Journal of Solid-State Circuits* (JSSC), considered the leading journal in the integrated circuit design field. The award is given for outstanding contributions to solid-state circuits, as exemplified by benefit to society, enhancement to technology and professional leadership.

Following his receipt of the BS (’89), MS (’90), and PhD (’94) degrees in electrical engineering and computer science from the University of California, Berkeley, Professor Chandrakasan joined the EECS faculty in 1994. While a graduate student in 1992, Chandrakasan authored a *JSSC* paper titled "Low-Power Digital CMOS Design" that brought the concept of the power-efficient chip to reality. The paper also became the second-most cited in the history of the *JSSC*. At the 1994 IEEE International Solid-State Circuits Conference (ISSCC), he presented a landmark paper focusing on a low-voltage/low-power chipset for a multimedia terminal.

Chandrakasan, who is also the former director of the MIT Microsystems Technology Laboratories, has made many pioneering contributions to the design of low-power digital and analog integrated circuits. Along with his students, he has demonstrated ultra-low-power sensor electronics, including low-power data converters, energy-harvesting ICs (vibration, thermal, and solar), sub-threshold digital electronics, and micro-power narrowband and ultra-wideband radios. His group has also demonstrated many low-power signal processing systems such as video compression and data encryption. These systems have featured adaptive power management concepts such as dynamic voltage and frequency scaling.

Chandrakasan, an IEEE fellow, has taken an active role in his field, serving as technical program co-chair for the 1997 International Symposium on Low Power Electronics and Design (ISLPED), for VLSI Design '98, and for the 1998 IEEE Workshop on Signal Processing Systems. He was the program chair for the IEEE ISSCC in 2003 and has been serving as the conference chair since 2010; ISSCC (a.k.a. the 'Chip Olympics') is widely recognized as the premier solid-state-circuits and systems-on-a-chip conference. He is a co-author of *Low Power Digital CMOS Design* (1995), *Digital Integrated Circuits* (2003), and *Sub-threshold Design for Ultra-Low Power Systems* (2006).

In 2009, Chandrakasan received the Semiconductor Industry Association (SIA) University Researcher Award. He was a co-recipient of several best paper awards, including the ISSCC Jack Kilby Award for Outstanding Student Paper (2007, 2008, 2009).

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