STATS ChipPAC?s fan-out wafer technology platform delivers high performance, highly integrated solutions in a wide range of package configurations

Medical Design Technology

STATS ChipPAC Ltd. (“STATS ChipPAC” or the “Company” – SGX-ST: STATSChP), a leading semiconductor test and advanced packaging service provider, today announced a new, wider range of packaging configurations in its fan-out wafer level technology platform that is able to address complex designs, shrinking lithography nodes and increased performance demands for mobile and consumer applications.

Increasing demand for more advanced electronic products with superior functionality, higher I/O density and increased performance in a smaller form factor is driving technology integration at the die and package level. Fan-out wafer level technology offers the ability to provide a higher number of interconnects than is possible with fan-in wafer level technology. The cornerstone of STATS ChipPAC’s fan-out wafer level technology platform is embedded Wafer-Level Ball Grid Array (eWLB). With over 100 million units shipped from its Singapore operation, STATS ChipPAC has established itself as the manufacturing and volume leader for this technology with capabilities in both 200mm and 300mm wafer formats.

“*As die sizes and lithography nodes continue to shrink, the challenge is to find the most efficient way to integrate more functionality and performance into a final solution. In order to address these complex challenges, advanced packaging is playing an increasingly vital role in functional integration. By combining eWLB technology with our Through Silicon Via (TSV) and Integrated Passive Device (IPD) technology we are achieving new levels of heterogeneous integration in a wide range of design configurations including small die, large die, multi-die, multi-layer and stacked packages*,” said **Dr. Han Byung Joon**, Executive Vice President and Chief Technology Officer, STATS ChipPAC.

eWLB is a powerful wafer level technology that has the design flexibility to accommodate an unlimited number of interconnects and is unconstrained by die size. This has allowed eWLB to meet the relentless form factor requirements and performance demands of the mobile and handheld market. STATS ChipPAC’s significant focus and investment in the evolution of this technology has resulted in an expanded range of package architectures. This includes single die, multi-die, ultra thin, System-in-Package (SiP) and three dimensional (3D) packaging, all with superior electrical and thermal operating characteristics. With its many technology attributes including a solid integration platform and a revolutionary structure which makes it inherently one of the thinnest package profiles in the industry, eWLB appeals to an increasingly broad range of market applications.

STATS ChipPAC offers a number of advanced package architectures which integrate eWLB with TSV and IPD. TSV technology enables the integration of semiconductor die fabricated in different technology nodes with diverse testing requirements. The short vertical TSV interconnections through the silicon wafer achieve greater space efficiencies for a smaller form factor and higher electrical performance. Passive devices such as resistors, capacitors, inductors, filters and baluns can consume 60% to 70% of available space in a system, subsystem or SiP package. Integrating TSV and IPD technology in an eWLB design delivers clear advantages such as advanced heterogeneous system integration, higher electrical performance and reduced form factor packaging.

Dr. Han continued, "*The ability we have to integrate TSV and IPD with eWLB technology opens up a wide range of possible design configurations for SiP and 3D packaging at the silicon level. This is an effective approach to system partitioning which offers our customers an overall better system performance*."

STATS ChipPAC will be presenting the latest information on eWLB, TSV, IPD and other innovative technologies such as fcCuBETM and die-to-die copper wirebonding for 3D packaging at the Electronic Components and Technology Conference that is being held May 31st to June 3rd, 2011 in Orlando, Florida.

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