TSMC disclose plans expansion in ?Mid-end? IC-packaging

Medical Design Technology

For years, TSMC has offered limited pieces of the backend puzzle, such as wafer bumping, wafer sort and wafer-level chip-scale packaging. It also develops other packaging technologies on a limited basis in order to understand the characteristics between IC design, manufacturing and packaging.

But TSMC and others hand off the bulk of the IC-packaging and testing requirements to the subcontractors. Now, however, TSMC is readying a new bumping facility and expanding its wafer-level chip-scale packaging efforts. And it will soon begin to offer silicon interposers and through-silicon-via (TSV) technologies for 3-D chips, which could be considered part of the backend process.

The move leaves some to wonder if the silicon foundry giant is gradually moving into the IC-packaging world, thereby competing against Amkor, ASE, SPIL, STATs and other subcontractors.

If not competing against the subcontractors, TSMC is stepping on their toes. **Rick Cassidy**, president of TSMC's U.S. unit, TSMC North America, said TSMC remains focused on the foundry market-and is not competing against the IC-packaging houses. ''*We're a front-end company*,'' he told EE Times.

Cassidy did say that the ''lines are blurring'' between some parts of the wafer manufacturing and packaging processes, prompting TSMC to invest and develop some technologies in the arena.

For years, TSMC has offered wafer-level bumping services. Some customers request that TSMC handle those functions as part of the overall manufacturing process. Other customers want the subcontractors to handle those functions.

Lee Smith, vice president of business development of subcontractor Amkor Technology Inc., does not view TSMC's chip-packaging efforts as direct competition. TSMC provides limited backend offerings; in contrast, the subcontractors offer a plethora of higher-end packaging and testing services, Smith said.

Smith also considers wafer-level bumping and wafer-level packaging a natural outgrowth of the front-end manufacturing process. Besides, wafer-level bumping is also a lower margin business, he said.

In 3-D packaging, the lines blur between manufacturing and packaging. However, Amkor has no plans to do ''the drilling and filling'' in terms of TSVs. That will be left up to TSMC and others.

Ultimately, Amkor and others will join forces with the foundries in TSVs. Working with foundries, Amkor will provide wafer thinning and other services in what is called a ''via-mid'' process.

Still, TSMC is expanding its backend efforts. At present, the company has two wafer bumping facilities, which are located in Hsinchu and Tainan. In those plants, it provides traditional and lead-free bump services.

This month, it will ramp up a new facility, BP2B/CP2B, in Tainan. The 12,000-square-meter plant can process from 200,000 to 250,000 wafers per month, said Marvin Liao, senior director of the backend technology and technology service division at TSMC.

TSMC is also in the process of qualifying its lead-free and new copper pillar bump technology at the 28-nm node. In copper pillar, the company initially devised a 140-micron bump pitch technology, but customers were not happy with the offering, he said. By year's end, the company will offer a 100-micron bump pitch technology, he said.

In another technology, TSMC ramped up its wafer-level chip-scale packaging production last year. It plans to move into 28-nm qualification by December. In that area, TSMC is targeting the mobile market.

In 3-D, TSMC will initially offer a silicon interposer technology. The company has provided samples, but production is not due until the end of 2012, said Shang-Yi Chiang, senior vice president of R&D at TSMC.

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