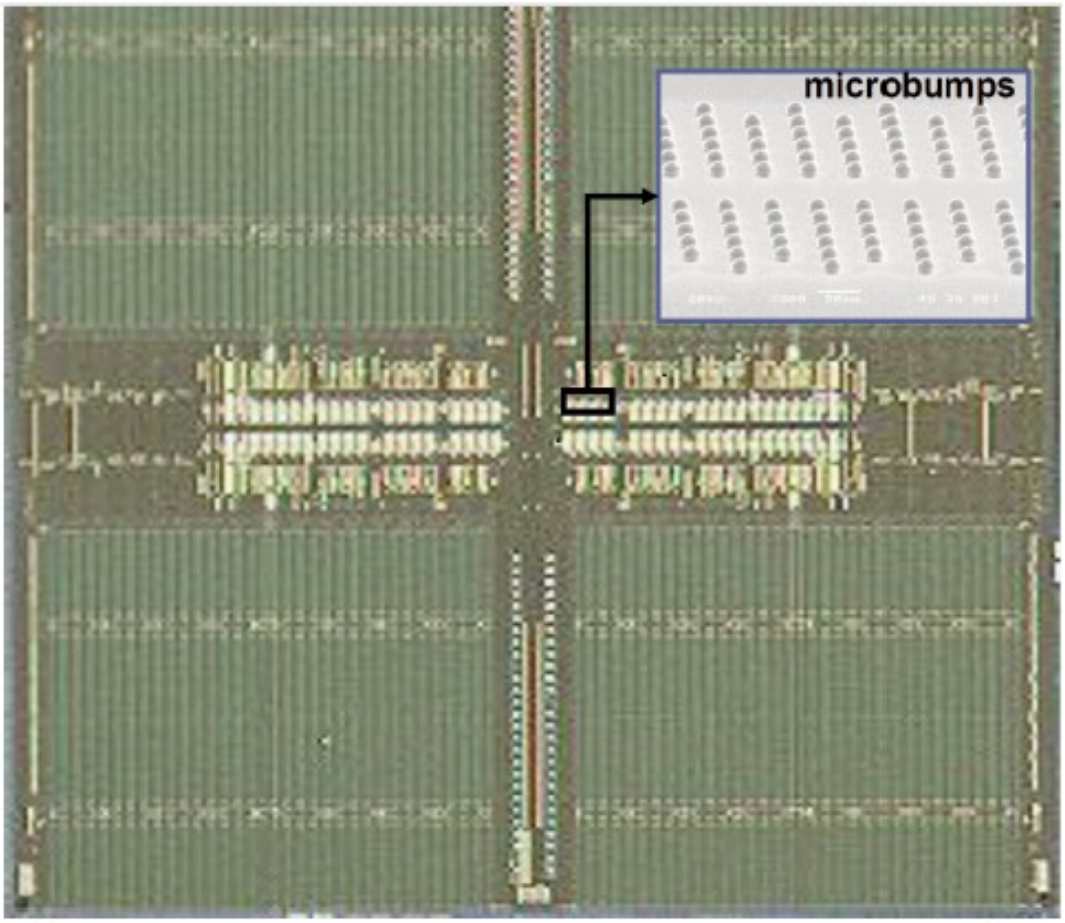
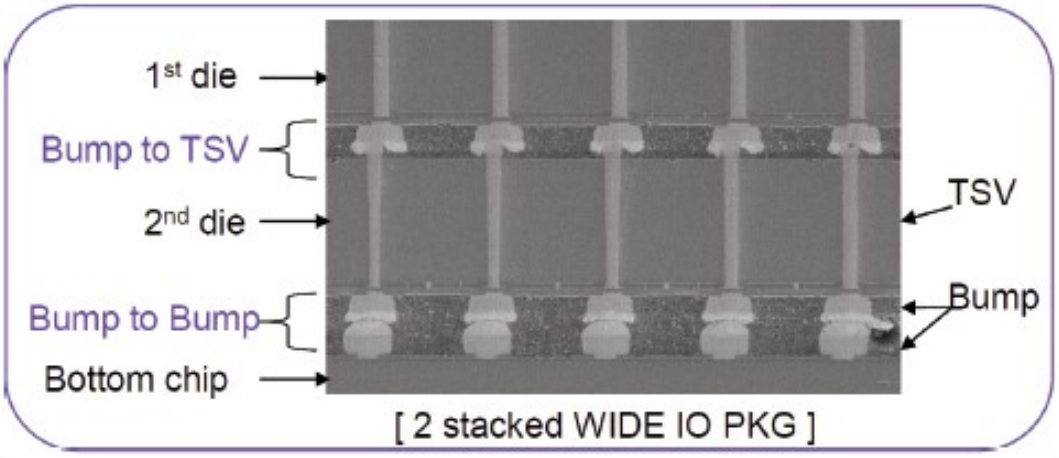
Samsung Wide-IO Memory for Mobile Products - A Deeper Look

Medical Design Technology

Earlier this week i-Micronews reported that Samsung has just announced wide IO DRAM for mobile applications (see the related articles here: Samsung develops mobile DRAM with wide I/O interface using 50 nanometer process technology [1] and At ISSCC 2011, Samsung announced 1Gbit DRAM in a 3D TSV package [2]).

Now let's take a closer look at what was said and what it means.





Wide IO DRAM memory for mobile products (Courtesy of Samsung)

Oh-Hyun Kwon, President of Samsung Electronics, in his plenary lecture at the IEEE ISSCC conference, shared their global motivation when he indicated that world-wide electrical-energy consumption in 2010 is estimated to be as large as 800TW•h. Samsung supports the concept that electronic products need "…efforts to replace conventional mechanical and other energy intensive parts by relatively energy-efficient semiconductor products" and they also support efforts to "…improve energy efficiency of the semiconductor devices themselves".

Looking at memory devices Kwon concludes that there are two categories: system memory and storage devices.

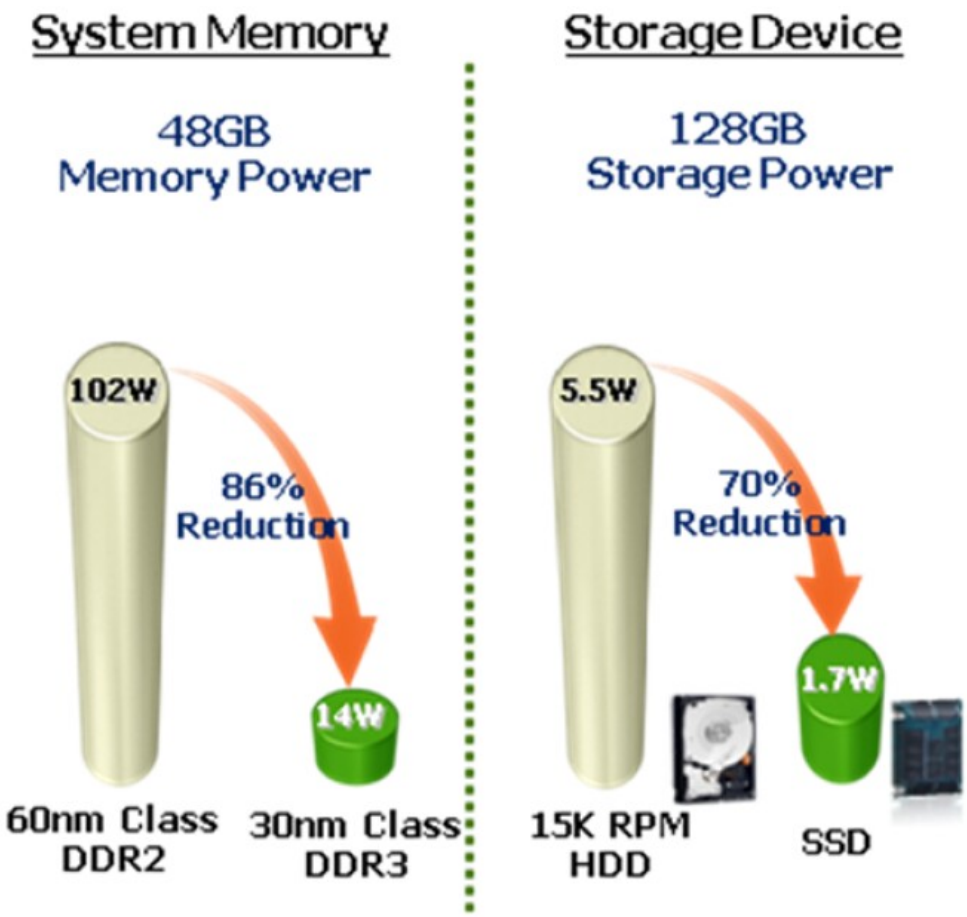
System memory devices must quickly process large amounts of data to keep up with enhanced processor performance in PCs and servers. "These days, low power consumption has become very critical as the power required by memory is a relatively large portion of that used in server and mobile applications. Especially as memory-intensive applications, such as cloud computing and virtualization, increase, energy efficiency is becoming more critical." Storage devices, such as Hard-Disk Drives (HDD), focus on very-fast storage of large amounts of data in a small physical area. "NAND flash memory has proliferated as the storage medium in music players since 2004. Now, it is being applied for storage in PCs and servers, due to its favorable characteristics of low power, high performance, high reliability, and small form factor. Solid-State Drives (SSDs), consisting of a controller and NAND flash memory, have been developed, and are beginning to replace conventional HDDs."

Power consumption of DRAM system memory has been driven by scaling. The smaller geometry available in advanced process technology required the application of lower supply voltages in DRAM devices, i.e. 3.3V for SDRAM, 2.5V DDR SDRAM, 1.8V for DDR2 SDRAM, and 1.5V for DDR3 SDRAM. "…power gating and the use of dual driver voltage per operation, have [also] contributed significantly to power optimization".

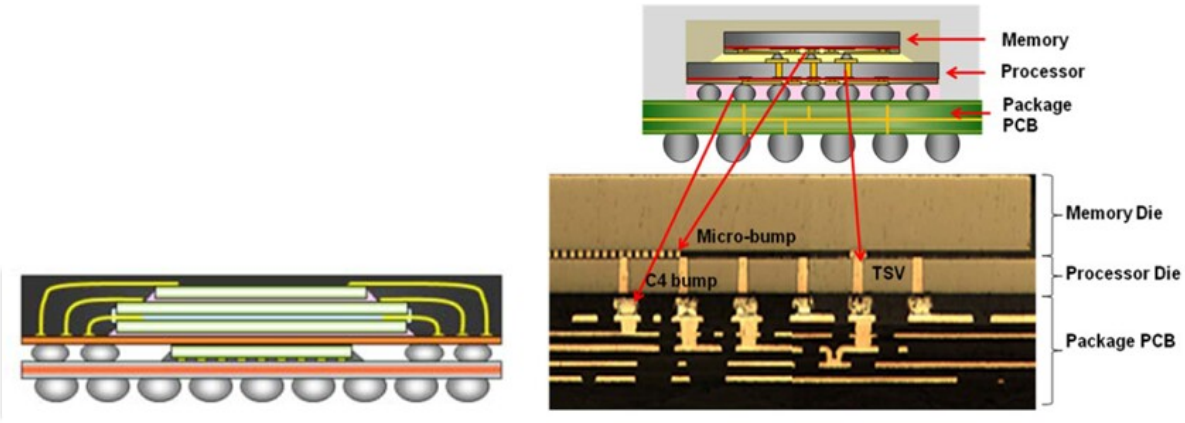
Due to the increase in technical complexity and the difficulty of equipment development, Kwon concludes that new approaches for overcoming such challenges will be necessary. "In 2011, 20nm process technology will be introduced, with 10nm and sub-10nm class technologies to be developed… the supply voltage in these technologies will decrease to 1.2V, 1.0V, and sub-1.0V …additional power reduction is unlikely without new technologies and new materials, because the definition of cell capacitors and cell-array transistors becomes more difficult as process technology enters into the sub-10nm range. In system memory, new technologies such as Wide IO, TSV, and optical IO … will be strong candidates in this process".

In storage devices, the focus is on reduction of power consumption by the mechanical parts (platters, spindles, arms) of the HDD because this is a significant portion of HDD total power consumption. Since SSDs do not have mechanical parts,

power consumption is determined solely by the semiconductor components, i.e the controller and the NAND-flash memory itself. Kwon reports that power consumption can be reduced 3.5 times by replacing a HDD with a SSD. Kwon also reports that the industry has now turned it sights to developing technology to reduce the power consumption of the controller and the NAND-flash memory. New NAND flash memories such as 3D-cell NAND (vertically-stacked cell – not to be confused with 3D TSV integration) and 3-bit or 4-bit per cell NAND are being developed to reduce the power consumption per bit.



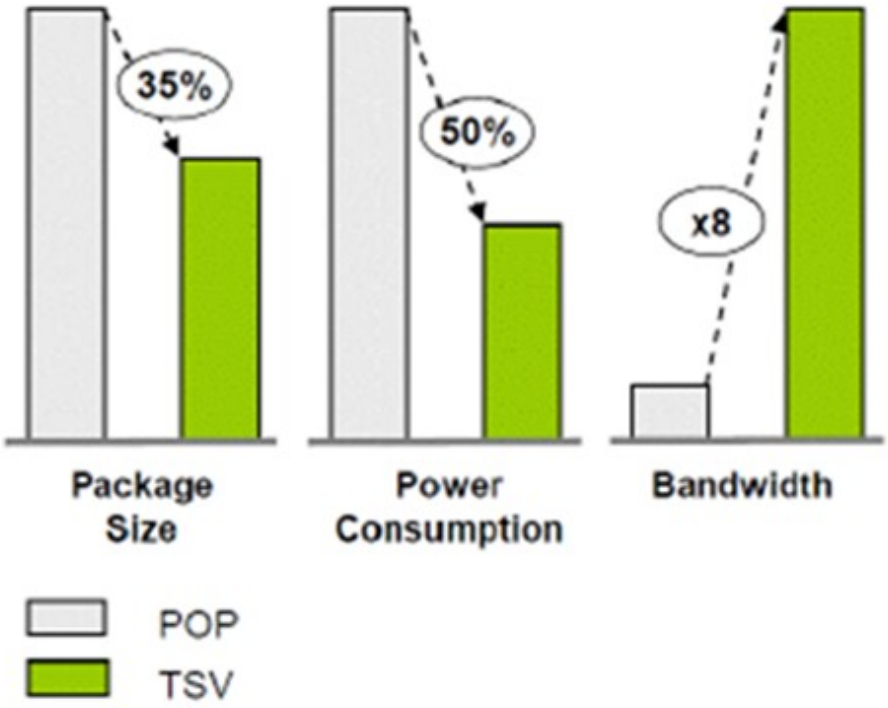
Looking more closely at the use of TSV technology as a means of reducing power consumption, Kwon compared a conventional 3D package using FC PoP with LPDDR2 memory (low power DDR2) to an equivalent SiP with wide IO memory. One can see the decrease in memory consumption is significant.



FC PoP TSV-SiP with wide IO DRAM

	Conventional 3D Package (FC-PoP) with LPDDR2	TSV-SIP with Wide IO memory
Memory I/O Power Consumption	176 mW	44 mW

It is this data that led Samsung to the more generic slide which shows the power consumption, package size and bandwidth advantages of TSV based technology.



Comparison of package performance: wire-bonding PoP vs wide IO interface with TSV (Courtesy of Samsung)

In related disclosure at the ISSCC, Samsung researchers offered more details on the

wide I/O memory in their technical presentation entitled “A 1.2V 12.8 Gb/s 2 Gb Mobile Wide I/O DRAM with 4 x 128 I/O Using TSV Based Stacking”.

Previous generations of mobile DRAMs used a maximum of 32 pins for I/O. The new wide I/O solution which has 512 I/O (up to 1200 total) pins can transmit data at a rate of 12.8-Gb/s. It is expected to replace low power DDR2 DRAM (LPDDR2) which runs at approximately 3.2-Gb/s according to Samsung. Following this wide I/O DRAM launch, Samsung is aiming to provide 20nm, 4Gb wide I/O mobile DRAM sometime in 2013.

Reportedly, "wide" parallel interfaces are more expensive to manufacture and package, but Samsung claims that by using the 1Gb memory chip with wide bandwidth, their customers can replace several smaller chips which results in reduced costs and higher performance.

The die area is 64.34mm2 (25% larger than 1Gb LPDDR2). The whole chip is made up of 4 symmetric partitions of 4×64Mb arrays, peripheral circuits and microbumps. To reduce power consumption and support high data bandwidth, I/O driver loading is reduced by adoption of 44×6 microbump pads per channel, which are located in the middle of the chip. The microbumps are 20×17µm2 on 50µm pitch. A fabricated TSV has 7.5µm diameter, 0.22 to 0.24Ω resistance and 47.4fF capacitance.

SOURCE [3]

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