STATS ChipPAC reports over 50% growth in flip chip business with more than 250 million units shipped in 2010

Medical Design Technology

With the rapid expansion of its flip chip technology offering and manufacturing footprint, STATS ChipPAC has been able to support the strategic growth of its flip chip customers. The Company's sizeable flip chip portfolio ranges from large single die fcBGA packages with passive components used for graphics, CPU and ASIC devices to smaller fcFBGA packages including single die, multi-die and stacked configurations that combine wire bond and flip chip technology within a single package.

During 2010, STATS ChipPAC continued ramping up production of its flagship Bond-on-Lead (BOL) interconnection technology which enables the reduction in flip chip packaging cost while alleviating stress and mechanical damage to low K and extreme low K (ELK) layers in silicon. To address a wider range of applications requiring higher Input/Output (I/O) densities, copper column bump was introduced in conjunction with the BOL design to provide customers with a cost effective, lead-free flip chip solution that is scalable to very fine bump pitches. In addition, a number of process innovations in areas such as bumped wafer thinning, advanced molding technology, and die and substrate handling were introduced to achieve thinner flip chip packages with higher yields.

STATS ChipPAC has made strategic investments in its flip chip manufacturing operations to support the growth of customer demand in recent years. Today, the Company offers wafer bump and sort services in Taiwan, Singapore and China with assembly and final test services in South Korea, Taiwan, Singapore and China.

"*We have had phenomenal growth in our flip chip business this year. In addition to our sustained leadership in packaging for the mobile market, we have diversified our flip chip technology portfolio and gained market share in the computing and networking markets. We have also expanded our foundry alliances to enable early development and qualification of flip chip packaging solutions for advanced silicon nodes. We are confident that these factors will provide us with a healthy growth trajectory going into 2011,*" said **Dr. Raj Pendse**, Vice President of Advanced Product and Technology Marketing, STATS ChipPAC.

Core enabling technologies such as copper column bump and fine pitch interconnection provide a seamless migration path into more advanced solutions such as Through Silicon Via (TSV) which require fine silicon-to-silicon and silicon-to-substrate interconnection. STATS ChipPAC's leading edge facility in Singapore is already active in the development of TSV technology solutions that provide a higher level of integration in a smaller form factor.

Dr. Pendse continued, "*While we focus on delivering the best flip chip solutions to our customers today, we are also taking a more holistic view of future market trends and selecting core technology elements that become building blocks for our future products. Copper column bump, BOL interconnection, advanced wafer thinning and thin die/substrate handling are examples of such technology elements which will find increasing use in our upcoming new product introductions.*"

SOURCE [1]

SOURCE [2]

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