Collaboration to Accelerate Development of 3D Stacked-IC Tech

Synopsys, a leader in software and IP for semiconductor design, verification and manufacturing, and the Belgian nanoelectronics research center, imec, announced they have entered into a collaboration to use Synopsys TCAD (Technology Computer-Aided Design) finite-element method tools for characterizing and optimizing the reliability and electrical performance of through-silicon vias (TSVs). The collaboration will accelerate the development of 3D stacked IC technologies.

While considered an emerging technology, 3D stacked IC complements conventional transistor scaling and allows multiple chips to be stacked and integrated into a single package. This technology reduces form factor and power consumption, and increases bandwidth of inter-chip communication by minimizing connections through the circuit board with high parasitic capacitance. As with other innovative technologies, 3D stacked IC introduces a number of new issues that can potentially affect its reliability and performance. The collaborative research to address these issues will take place at imec, where silicon wafers with test structures will be manufactured and tested, and Synopsys' TCAD tools will be used to model the TSVs in the chip stacks to optimize 3D stacked IC performance and reliability.

"We consider the availability of Synopsys' silicon-proven finite-element method tools to be an integral part of deploying 3D stacked IC technology. This collaboration will speed up the development of through-silicon via technologies and will in turn facilitate the adoption of 3D stacked ICs in the semiconductor industry," said Luc Van den hove, president and chief executive officer of imec.

"This collaboration with imec affords us the opportunity to validate Synopsys' industry- leading TCAD simulation tools for addressing the emerging 3D stacked IC technology. Imec is an ideal collaboration partner for this effort given its excellent research facilities, industry focus and expertise," said Howard Ko, general manager and senior vice president of the Silicon Engineering Group at Synopsys.

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Further information on imec can be found at www.imec.be [2].

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