Think parallel

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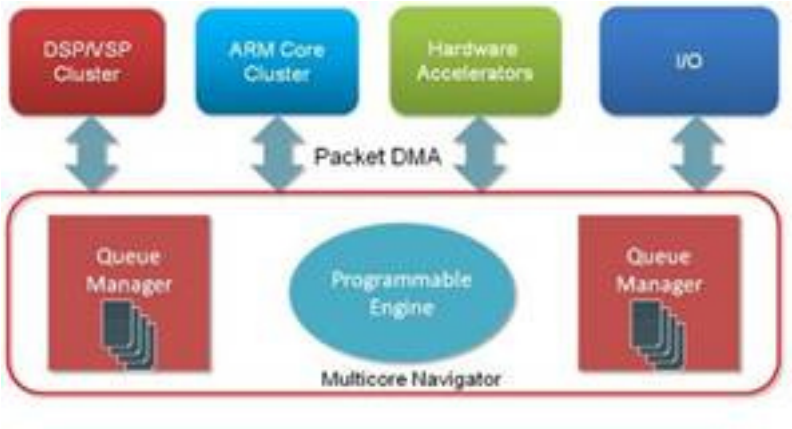
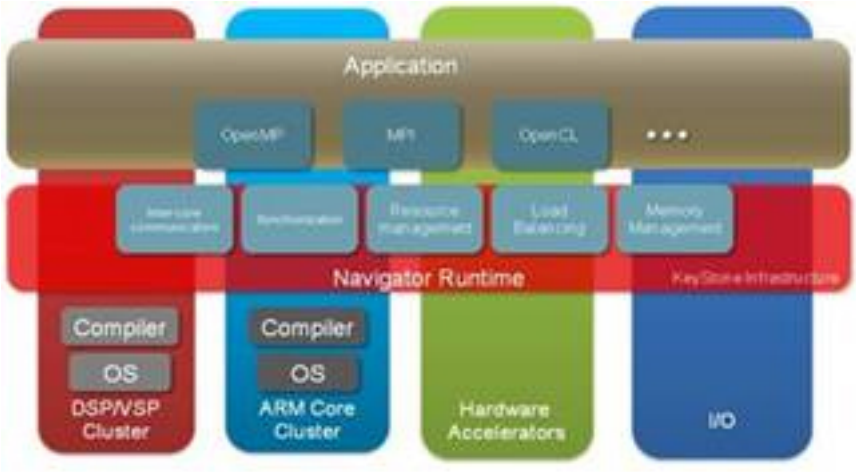
Does multicore have you thinking parallel? It's true that multicore processors require a new level of parallel programming skills, and with our KeyStone multicore SoC, a high degree of parallelization is achieved through architecture parallelism and memory parallelism, as well as instruction level parallelism.

Our Multicore Navigator provides architecture parallelism with a unified interface for cores, accelerators and I/O using hardware queues and packet DMA for communication, data transfer and task management. This provides common communication methodology for all IP blocks. Traffic routing, IPC, resource management, scheduling and load balancing are managed by the Navigator by leveraging built-in programmable engine designed to optimize and expedite data flow. Task parallelization can be offloaded using the Navigator to ease multicore programming effort. The picture below shows the Navigator enabling KeyStone architecture parallelism.



Navigator Runtime is a thin and scalable software layer that extends the Navigator to achieve a higher level of parallel programming performance providing increased scalability, portability and efficiency. The picture below shows a programming model on KeyStone SoC. The combination of the Navigator and Navigator Runtime offers a powerful and unique solution to the challenges of multicore programming.



What are your thoughts on parallelism?

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