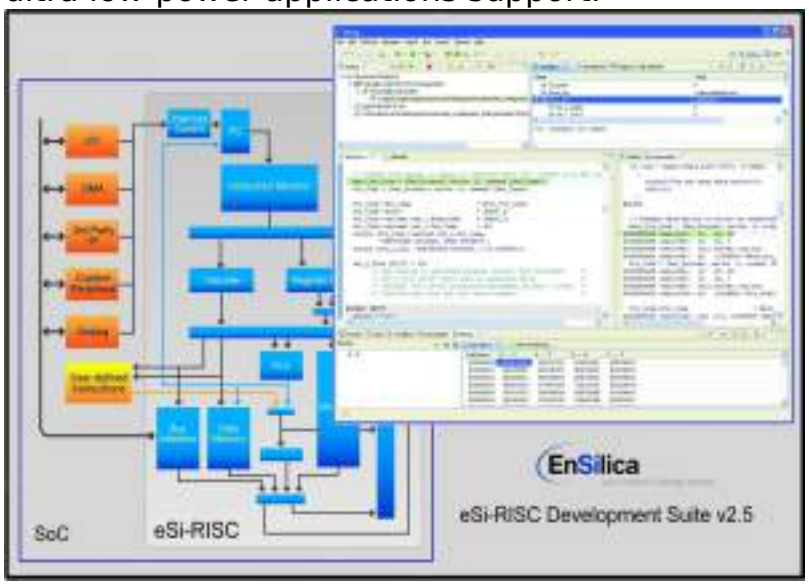
EnSilica launches version 2.5 of its eSi-RISC Development Suite

ECN Europe

EnSilica [1] has launched the eSi-RISC Development Suite v2.5, a new version of its complete development environment for evaluating the EnSilica family of eSi-RISC highly configurable and low-power soft processor cores and the development of embedded applications. The eSi-RISC Development Suite v2.5 features new capabilities for multicore support, significantly enhanced compiler performance and ultra low-power applications support.



[2]

Picture: EnSilica

With the increasing trend towards multicore eSi-RISC designs such as dual core secure processor applications and Posedge's innovative 7-core Residential and SMB Gateway, the eSi-RISC development Suite v2.5 now provides JTAG debug and control over all processors in the JTAG chain. In addition, optional load locked and store conditional instructions have been added to the instruction set to support multicore systems.
SOURCE [3]

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[2] http://ecneurope.files.wordpress.com/2011/10/311011-ensilica.jpg
[3] http://ecneurope.wordpress.com/2011/10/31/ensilica-launches-version-2-5-of-its-

esi-risc-development-suite/