

Optimizing high-speed, embedded memory interface designs

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Addressing considerations in high speed bus designs for a healthy “data eye”



Designers of energy-efficient, high-speed memory subsystems for small form factor or power-sensitive embedded and wireless products are often making the shift from traditional DDR2/DDR3 to low power (LP) DDR2/DDR3 memory solutions. This is largely in response to the ever-challenging power reduction requirements, which reflect user system standby and wake-up time expectations.

The interface buses for these low-power memory devices need to operate reliably at data transfer rates approaching 2Gb/s in virtually any environment—regardless of temperature variations and EMI noise interactions. Consequently, the signal integrity of the so-called signal data eye must be as robust as possible. To ensure this, careful attention must be paid to PCB trace layout topology and stacking, as well as decoupling and impedance matching for LPDDR2/LPDDR3 interfaces with system-on-chip (SoC) processors.

Difficulties with interface designs are often magnified due to board size and shape constraints, along with time to market pressures, which can create significant topology validation challenges when implementing LPDDR2/LPDDR3. Extensive validation through simulation using DRAM and SoC supplier IBIS or HSpice models, along with detailed PCB signal trace parasitic model files, is no longer optional. Design simulation using these models must be completed and critically reviewed before PCB generation to avoid problems that could result in missing a product market window.

Designing a high-speed bus for LPDDR2/LPDDR3 encompasses all of the considerations listed below. Fortunately, some of these can be eliminated or simplified for typical embedded high-speed memory subsystems.

Critical design elements for improving signal

integrity:

Basic signal trace properties

- **Total**

length

- **Effective**

length

- **Length to**

terminations

- **Min/max trace lengths for a group**
- **Trace widths**

- **Via counts, layer changes**

Impedance matching

- **Single-ended impedances**
- **Differential impedances**

**Neighbor
spacing**

- **Spacing to adjacent nets (broken down by region)**
- **Serpentine spacing to**

self

Plane references

- **Signal reference**

plane

- **Plane split**

crossings

- **Distance to plane edge**

Signal return paths

Decoupling capacitor values, type, and placement

Embedded and wireless DRAM designs are often simple point-to-point configurations with one SoC controller interfaced with one DRAM. This often results in worst-case bus signal trace lengths that are less than 5cm. These relatively short bus trace lengths typically allow termination to be avoided altogether, at least for data transfer rates below ~1Gb/s, depending on the actual signal trace topology. This is governed by the ratio of signal rise time to the transmission line propagation delay time. At higher data transfer rates, transmission line principles need to be applied when designing and performing the recommended signal integrity simulation and analysis on the interface buses.

With data rates increasing, signal trace length matching is a growing concern for DRAM designs. Closer matching of trace lengths will reduce signal edge skew or delay and help preserve margin within the overall bus timing budget. Trace length matching is most critical within signal groups such as data bus byte lanes (DQ0-7, DQ8-15, etc.). Since the bidirectional data strobe (DQSx) associated with each data

byte lane of the data bus is also a critical element of the byte lane functionality, it should be included in a review for signal group trace length matching. Signal skew due to any trace length mismatch within a group will have a negative effect and reduce margin in the overall timing budget. Table 1 illustrates an example of signal skew time induced by trace length mismatches within byte lanes.

Table 1. Signal skew/delay within byte lanes

DDR_DQS0	21.822	DDR_DQS1	20.970	DDR_DQS2	21.701	DDR_DQS3	21.896
DDR_DQS_N0	21.770	DDR_DQS_N1	21.068	DDR_DQS_N2	21.708	DDR_DQS_N3	21.940
DDR_DM0	19.876	DDR_DM1	20.297	DDR_DM2	21.252	DDR_DM3	20.271
DDR_DQ0	20.791	DDR_DQ8	20.689	DDR_DQ16	19.901	DDR_DQ24	22.323
DDR_DQ1	20.102	DDR_DQ9	20.740	DDR_DQ17	19.950	DDR_DQ25	19.927
DDR_DQ2	20.140	DDR_DQ10	20.136	DDR_DQ18	20.403	DDR_DQ26	21.126
DDR_DQ3	20.064	DDR_DQ11	20.101	DDR_DQ19	20.196	DDR_DQ27	22.283
DDR_DQ4	20.120	DDR_DQ12	20.887	DDR_DQ20	19.951	DDR_DQ28	20.443
DDR_DQ5	21.534	DDR_DQ13	21.821	DDR_DQ21	21.707	DDR_DQ29	21.135
DDR_DQ6	20.781	DDR_DQ14	20.131	DDR_DQ22	19.863	DDR_DQ30	21.280
DDR_DQ7	21.388	DDR_DQ15	20.682	DDR_DQ23	19.966	DDR_DQ31	20.920
min (mm)	19.876	min (mm)	20.101	min (mm)	19.863	min (mm)	19.927
max (mm)	21.822	max (mm)	21.821	max (mm)	21.708	max (mm)	22.323
delta (mm)	1.946	delta (mm)	1.720	delta (mm)	1.844	delta (mm)	2.396
%delta	8.918	%delta	7.881	%delta	8.497	%delta	10.733
delay (ps)	14.148	delay (ps)	12.502	delay (ps)	13.409	delay (ps)	17.418

Source: Micron®

Signal Timing Skew within DQ Groups

To some extent, serpentine signal trace patterns can be used to add a small amount of length to shorter traces and improve overall length matching within a signal group. However, as transfer rates approach 2Gb/s, the effects of self-coupling can come into play on the serpentine traces. Therefore, minimum spacing requirements between these features also may apply.

When routing many signals within a small space, some signal path layer changes are unavoidable. Each via used for this purpose adds a delay (as much as 20ps) to signal propagation. Therefore, this delay must be included when assessing the overall skew that the signals will experience relative to one another.

Many signal trace routing complications are reduced in cases where package-on-package (PoP) configurations can be used because DRAM bus trace routing through the PCB to the SoC is eliminated. This is typically a much cleaner environment from a signal integrity standpoint because the signal traces are much shorter and entirely contained within the package substrates of the SoC and DRAM PoP stack.

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For higher-density memory solutions, point-to-multipoint bus configurations (one SoC memory controller interfaced to multiple DRAM components) are required. This generally results in longer signal trace lengths and transmission line stubs to the unselected products. For LPDDR3 devices, a new on-die termination (ODT) feature has been added to the DQ receiver design to permit better impedance matching during DRAM WRITE operations on the more complicated, multipoint topologies when operating at higher speeds. ODT can be dynamically engaged by the memory controller to better terminate the selected DRAM component data bus. Many SoC memory controllers also incorporate this in their DQ buffer designs for use during DRAM READ operations.

This option helps meet the ideal scenario of impedance matching:

$$R_{ON} = Z_O = Z_T *$$

Where,

R_{ON} is output impedance of the transmitter driver,

Z_O is the characteristic impedance of the trace transmission line as it travels through various layers of the system PCB,

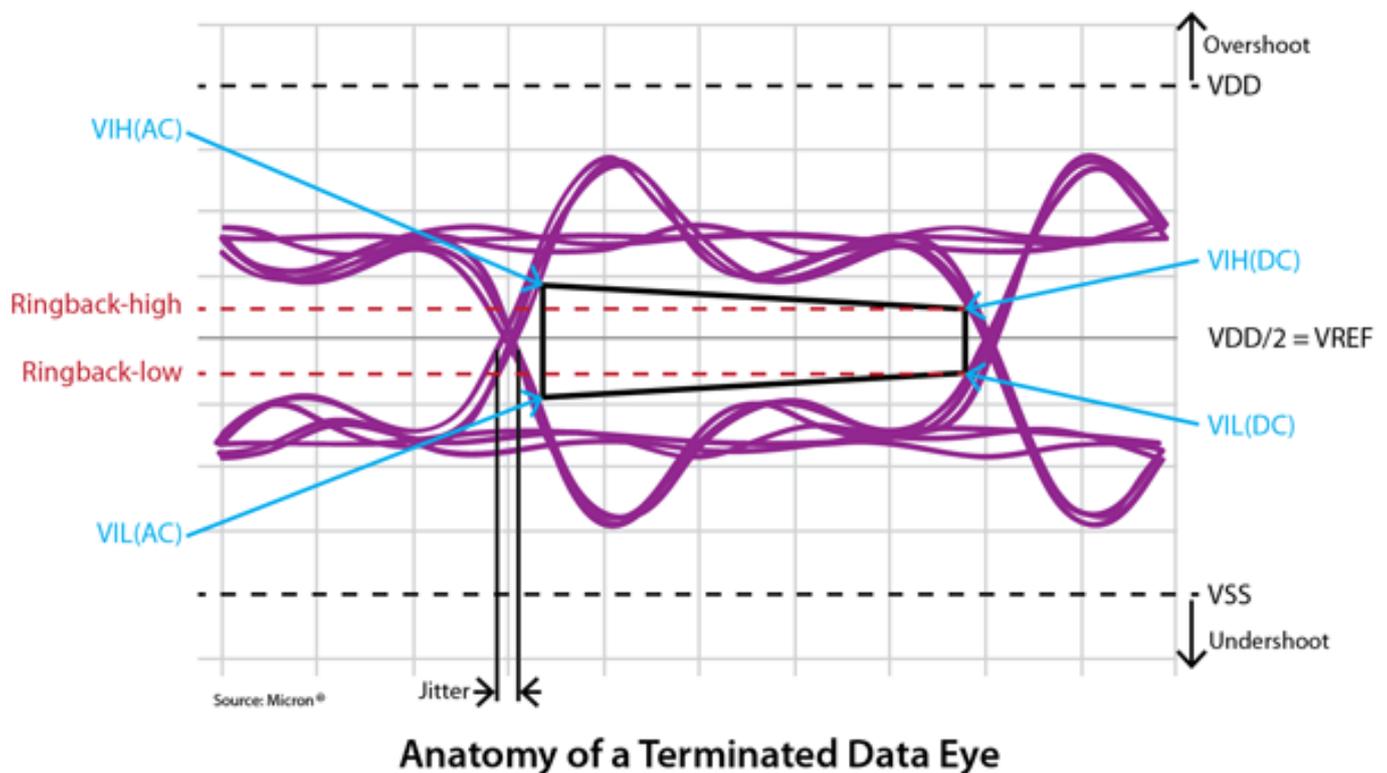
Z_T is the termination impedance of the receiver (provided by ODT or termination resistors placed in the signal trace).

** In practice, R_{ON} is often set slightly lower than Z_O , and Z_T is often set lower than Z_O for power savings.*

The LPDDR3 and SoC controller typically offer several values for R_{ON} and ODT for Z_T to accommodate this. Having the ODT feature available onboard the DRAM and SoC controller eliminates the space required and cost involved with placing discrete termination resistors on the PCB. Of course, any time termination is utilized for signal integrity optimization (provided by either ODT or discrete resistors), additional power consumption will be incurred.

The overall quality (or “health”) of the data eye diagram will depend on how much timing and voltage margin the bus interface signals have with respect to the DRAM and SoC product specifications. Some of these parameters are highlighted in the example signal eye diagram in Figure 1.

Figure 1. Anatomy of a terminated data eye



Signal integrity simulation and analysis tools are needed to verify that the data eyes for a proposed design are as robust as possible.

- IBIS or HSpice models for the memory and SoC controller receiver/transmitters (available from the product suppliers)
- BRD (or similar) model file exacted from the PCB layout
- Simulation environment suitable for signal integrity analysis
 1. Online bus simulators for first-order data eye evaluations(available from some suppliers)
 2. Commercially available simulation tools for more detailed analysis

With earlier DDR SDRAM devices, the address and command buses were somewhat less critical than the data bus from a timing and signal integrity perspective. This is because on earlier DRAM products, these buses operated with a single data rate protocol, while the data bus operated at double data rate. To reduce signal count, LPDDR2/LPDDR3 products operate with a combined address and command bus running at double data rate. Therefore, these buses need to be designed more carefully from a signal integrity standpoint.

Taking these primary considerations into account when designing a high-speed memory interface will increase the probability of success with the first PCB revision. For more in-depth coverage of the considerations presented, refer to major memory and SoC supplier web sites for technical notes and data sheets, including <http://www.micron.com/products/support/technical-notes> [1].

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