Roundtable: What new electronics packaging materials or techniques do you expect to gain popularity in 2013?

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Anindya Poddar, SC Packaging, www.ti.com [1]
Customers are demanding smaller, thinner, faster and more power efficient semiconductor solutions, especially for mobile applications, consumer electronics and the growing “Internet of Things.” Substrate advancements can help address these needs. New techniques are delivering materials with lower expansion and higher stiffness, resulting in thinner and/or coreless packages with reduced warpage. This will play an important role in improving Package on Package (PoP) adoption. Copper pillar is also benefitting from substrate advancements, and will continue to gain popularity. Copper pillar technology drives down the size and cost of semiconductors, providing higher current carrying capabilities in embedded processing, wireless, and power products.PoP solutions will evolve to TSV stacking for improved bandwidth as the industry matures and continues to identify solutions for more cost-effective TSV implementation.Increased integration will drive innovations in thermal management as increased power density and hot spots begin to impact system reliability. Newer materials for increased electrical, thermal performance, reliability, reduced package dimensions and cost will also see more applications. For high voltage and harsh applications, material chemistries that can withstand stringent breakdown strength and long-term exposure to elevated temperatures will experience increased growth. And finally, we see continued adoption of copper wire bonding as an alternative to gold. High-volume manufacturability has been proven, and the technology provides superior electrical performance with significantly higher electrical conductivity and lower operating resistance. These attributes improve performance in high-speed digital, high-current mixed signal, and power management applications.

Dan Ashley,Nordson ASYMTEK, www.nordsonasymtek.com [2]
New manufacturing techniques for underfilling package-on-package and chip scale packages in mobile devices will gain in popularity in 2013. Underfill is necessary to protect the solder joints and prevent these packages from damage. Presently, RF shields are soldered to the PCB to cover the package prior to underfilling. The shield makes it difficult for dispense heads jetting the fluid to access the critical areas around the packages where the fluid needs to be placed, lengthening process time. Each shield must be designed with holes immediately above each package to allow the underfill to pass through the RF barrier. If there are too many holes, or the hole diameter is too large, the RF waves will breach the shield, making the shield ineffective. If the shield has no access points, the capillary flow necessary for the underfill process will be impossible. Jetting underfill before the shield is attached saves time. In addition, design engineers are not limited by package placement to accommodate shield holes and higher density board population is possible. Production is faster, thereby producing more units per hour. With this method, a secondary solder paste station has to be added to the line to attach the shield. Because the board is already populated, a dispense system, rather than a screen printer, is usually used and a secondary reflow station is required. Although initial equipment costs will be higher, the benefits that come with added PCB design flexibility and increased UPH will drive the popularity of this method.

Tim Going, StratEdge Corporation, www.stratedge.com [3]
In 2013 we think you'll see a big increase in the use of high power dissipation packages designed specifically for gallium nitride (GaN) devices. GaN has 8x the power density of gallium arsenide (GaAs) and thus is driving these new designs. What's unique about these packages is the use of a base material that has high thermal conductivity and has a coefficient of thermal expansion that is well matched to the semiconductor device. The material we use is a copper-molybdenum-copper (CMC) laminate in the ratio of 1:3:1. Packages can be designed for frequencies from DC–63 GHz. GaN packages come with either a flange (bolt hole) so they can be bolted down or flangeless so they can be soldered to the board. Several different standard packages have been introduced for both discrete transistors and MMICS. Copper-based packages will be used for the highest power

requirements. Copper allows the heat to dissipate better so the junction temperature of the chip is lower and the chip can run colder, which increases the chip's efficiency. However, with pure copper, you are limited to very small packages of 1mm square or less due to the difference in the coefficient of expansion between the die and the copper. CMC is a more reliable long-term solution because of matched thermal coefficient of expansion. The CMC package can handle the same amount of power as pure copper, but might be slightly less efficient as it won't run quite as cool.

Christian Miraglia, Fujipoly, www.fujipoly.com [4]
The ever increasing power density of electronics poses the important need for addressing thermal issues at packaging. While some efforts are made at the packaging level to help with heat transfer, finding an appropriate thermal solution is ultimately the customer's choice. One issue that customers face is that most packages have a relatively high thermal resistance from junction to case. This can become somewhat of a thermal bottle neck. Certain packages use metal lids and even ceramics but plastic packages still seem to be the most common. The use of higher thermally conductive packaging material and improved level one TIM's will help to ensure heat is released from the package and onto the heat sink. Another issue impacting heat transfer is engineers are limited by the small die size compared to the package itself. Many customers assume the entire surface area of the package will have even heat flux. In reality this is not the case, most dies are actually significantly smaller than the package, with the exception of open dies and chip scale packages. This often leads to thermal models that vary dramatically from the real world. Ideally, a heat spreader is included in the IC package to reduce the power density over the surface of the package. Even though this is not a new idea - a quick search on Google will show all types of patented integrated heat spreader schemes - the option is more common in very high power devices such as FPGA and processors, than in standard packages. At the end of the day the thermal solution is exclusively the customer's decision. Designers that have had to find a way to thermally interface an IC to a heat sink have found themselves analyzing various stresses more than temperature gradients. Newer robust packages and solder pads will certainly make this choice easier on them in the upcoming year.

Links:
[1] http://www.ti.com
[2] http://www.nordsonasymtek.com
[3] http://www.stratedge.com
[4] http://www.fujipoly.com