Roundtable: What must designers of portable devices do to deal with power and performance demands?

What must designers of portable devices do to keep pace with increased power and performance demands?

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Designers must focus on power conservation while carefully considering power consumption and efficiency. For many years, the focus has been on reducing the power consumption of the electronic components and maximizing the efficiency of power conversion circuits. While these are worthwhile efforts, continued improvements are delivering less impactful improvements to a portable device's battery life.Focusing on power conversation involves a clear understanding of the usage profiles for the end product and an in-depth understanding of the major power consuming electronics. Then, by analyzing the power consumed by each device sub-system during a usage profile, methods can be devised to conserve the power consumed throughout each element of a usage profile. These methods often require improvements to software and resource utilization, in addition to some minimal hardware that may be required to allow the "power-down" of device sub-systems or adjustment of voltage levels. In products where the usage profiles not well defined, it may be beneficial to add power monitoring circuits so closed loop power conservation techniques can be implemented. By carefully crafting a complex system of optimized software and hardware circuitry, the power consumed by a portable device can be greatly reduced without significantly increasing the device cost or negatively impacting the user experience. Developing power conservation techniques, such as above, can be tedious and time consuming, but often result in a clear competitive advantage.

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An integrated, system-level approach is now the key to managing energy consumption during all the possible operating scenarios of smartphones, tablet computers and other portable electronic devices. The task is now so complex that

discrete analog power management components with separate digital controllers are not viable. They're too expensive in bill-of-materials, product assembly and printed circuit board real estate. What's more, they can't come close to delivering the performance or functionality of a dedicated power management IC (PMIC) that operates with an application processor at the system level.Today, in a single 8x8mm BGA package just 1mm high, PMIC makers are now packing multiple multi-mode DC/DC converters, some of which can be connected in parallel, that deliver over 12 Amps in total. They are integrating multiple LDO regulators, multiple GPIO pins, PWM drivers for LEDs, power and rail switches, and system-level monitoring, complete with watchdog timers. Some advanced devices run at 6MHz or more to help minimize the size of external components too. Compare this with discrete circuits, which are rarely effective above 1MHz. PMICs may also have a wide input voltage, running from everything from a single lithium ion battery cell to a USB or other 5 Volt power supply.Equally important, some PMICs come with software utilities that allow flexible experimentation, optimization of power sequencing and control, and the opportunity to create end-product differentiation.


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The simple answer to this question is to look for lower power devices to design into systems. However, the true picture is a little more complicated. Battery life is dependent upon the energy consumed by a system over its lifetime – energy consumption is the product of power consumption and time. Most MCU-based systems spend much of their time in a standby or sleep state during which power consumption is minimized to extend a battery's operating life or otherwise reduce energy costs. When woken up for the MCU to carry out a task or series of tasks, it may be preferable to have the system use more power for a shorter period of time, rather than less power for a longer period. This is one of the reasons why relatively powerful 32-bit processors can be more energy efficient than their seemingly lower power 8-bit and 16-bit rivals. In other words, careful choice of MCU can increase system performance and reduce energy consumption at the same time. Another important key consideration is how often the MCU needs to wake up. Choosing an MCU in which peripherals operate or communicate with each other without MCU intervention via a peripheral reflex system - utilizing a bus that carries both data and control signals - can result in a dramatic reduction in energy consumption over time. Such processors may consume only 25% of the energy of other so-called 'low power' MCUs.


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As portable electronic devices become smaller, more mobile and increasingly multifunctional, they require more advanced pressure vents and acoustic vents. Today's smartphones, e.g., are increasingly complex devices with ever-expanding functionality that are being used by more people every day for longer periods of time in an expanding diversity of operational conditions. Smartphones, handheld computers and scanners, two-way radios, cameras and other devices all require improved venting solutions in less space for superior acoustic performance and improved durability.Through comprehensive testing, Gore has identified several problems — liquid intrusion, particulate contamination, variations in pressure and corrosion — that require protection. To address these, we developed protective vents using expanded polytetrafluoroethylene (ePTFE) membranes with a node-and-fibril construction that allows gas molecules (air) to pass through while completely repelling liquids and solid particles. Obviously, the creating the best product is something we strive for, but we've also found that providing engineering support to our customers is equally as important as designing the product itself. Thisinteraction enables us to work with OEMs to address the many variables that can occur in various design scenarios. These collaborative efforts allow for the achievement of new levels of acoustic performance with reliable protection against dust, liquids, pressure differentials, and other demanding environmental conditions.


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Battery life improvements within portable devices, such as notebooks and medical equipment, have been driven primarily by processor vendors. Although there have been some holistic efforts, most power savings have come in the form of more dynamic control of the processor clock, core voltages, and suspend states. All of this dynamic power management has been limited to the processor and in some cases, the chipset. It does not extend into the system because each system has a unique set of requirements or characteristics that cannot be controlled by the CPU manufacturer. System designers must start taking advantage of the power management capabilities realized by dynamic programmable power management systems. Dynamic control of the whole power system can lead to greater than 10 percent extended battery life. Very few systems on the market enable "voltage dimming" where the 5V and 3.3V supplies are reduced to 4.8V and 3.1V depending on the state of the system, yet doing so would lower the power consumption by a cumulative 10 percent in these lower performance states. Extending the number of “power domains” (power rails) also allows the power system to optimize each subsystem or to completely shut it down. The cost per rail has been dropping, and dynamic programmable power systems now exist which meet the needs of portable system standby power requirements. The power system must get smarter and become part of the larger software controlled system

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To keep pace with the increased power and performance demands for today’s portable devices, designers should be aware of the role material selection plays in helping to meet these requirements, especially when faced with the accompanying challenge of creating smaller, more lightweight designs. High performance plastics are now available that can deliver an excellent balance of the desired properties and performance. For example, as devices get smaller and yet more powerful in terms of screen brightness, battery life and the number of antennae, designers need to consider thermal management; attenuation or clarity of antennae signals without interference; the protection of the valuable electronics inside the device and, of course, style and aesthetics. The selection of materials is critical when seeking to optimize style and performance, as well as the desired level of design freedom to support competitive differentiation of the device. Beyond meeting base requirements, the materials also need to be “smarter,” in some cases, able to multi-task by incorporating several performance requirements into one material, rather than using a combination of materials to deliver the desired effects.For example, designers may wish to consider whether the frame of a device (that provides mechanical stiffness and durability) could also be its antenna? Similarly, could the cover of a device also help it to dissipate the heat that is generated? Or kill bacteria at the same time? Can the touchscreen of the device not only enhance brightness but also avoid fingerprint smudges? Designers now have a wider array of plastic material options to choose from that can deliver performance, aesthetics, design freedom, and in some cases, more sustainable solutions achieved by consolidating parts, with intelligent designs enabled by high performance plastics.

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Mobility is important factor in almost everyone’s life, with the help of the technological progress many desktop devices have been miniaturized to handheld forms. With high Expectations, portable devices performance is expected to equal desktop devices. Mobile functions like GPS, acceleration sensing and long lasting power supply are a must for many mobile applications – proving that functionality needs to be at a higher level. This leads to increased power and performance requirements within limited space and weight. Designers must tackle the problem from different angles. Power requirements to the system must be kept to a

minimum, in most cases this means challenging the customer to keep system requirements to a minimum. This is a difficult task but very helpful for the devices power budget, helping keep the product simple, easy to use and deliver a stable and reliable performance. Secondly, designers must keep pace with advanced power management technologies, using both integrated solutions and discrete components. Advanced silicon technologies reduce power demands, increase integration level and improve power conversion efficiencies. Uses of low-power memory solutions, newest technologies for RF communication, batteries, power conversion and microprocessors help get power demand to a minimum. Boost/buck converters have better efficiency, selecting inductors with higher Q-value helps wasting less energy as heat. Lastly, the most demanding task is Designers taking care to design a smart system. In hardware/firmware domain, designers need to plan and define elaborated working states with different user case scenarios and power consumptions. For example, states like off/hibernate/deep sleep/idle and standby are solutions which set the basis for a clever design. Further, it makes sense to manage the device in different power modes, i.e. separate power IC's could be used in combination with a clever local PSU design to support modes where most of the system components are shutdown completely or put into an ultra-low power mode. Good designs make use of dynamic voltage technologies, where many internal parameters – frequencies and temperatures – are measured and the voltage is regulated accordingly in contrast to constant voltage supply where excess voltage is converted into heat. On the Software side advanced power management techniques as provided by the system should be used. Examples are dynamic frequency scaling, core voltage control, leakage management. Keeping CPU frequency down by using multi-core processors and making use of hardware accelerators is a perfect method to save power. Finding an optimum Design between increased power and performance demands and the rest of the product requirements like size, cost, features and usability gets more challenging and needs lots of intelligence and collaboration within a Design Teams to keep pace with that challenge.

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[8]The portable power management unit (PMU) provides design challenges not seen in other PMUs due to the mobility aspect of the end product. The target market of smart-phones, tablets and other mobile devices require highly efficient power management systems. The requirement stems from the desire to have longer battery lifetime while still supporting load-heavy applications. To do this effectively the efficiency targets need to be aligned with the system load profiles in the different system operating modes. This allows target peak efficiency over the full use-case scenario. The efficiency targets reach from the architecture of the

power providers such as linear dropout (LDO) regulators and switched-mode power supplies (SMPS) to the internal reference systems, the clock systems, and the lowest power operating modes of the chip. Designing for pre-regulation in the system is paramount to the optimization of power dissipation of the chip and the system. This leads to the integration of more and more SMPS regulators into the PMU and the design of LDO regulators, which require very low dropout. In addition to efficiency requirements, component size and height are important considerations for the ever-shrinking board, and the market trend towards thinner products. This impacts the external component choice imposing height and area requirements on inductors and requires innovative solutions to implement cap-less or remote cap regulator solutions without impacting performance. The final challenge in this low area highly integrated solution is control of chip and board thermal dissipation. To support heavy load applications, the PMU needs to monitor the die temperature to ensure that overheating doesn’t occur. Again, load scenarios are especially important to tackle this requirement and to have the right tradeoff in design between die area and peak efficiency.In summary, the requirements for portable PMUs are: high load, high efficiency, high integration, thermally viable, and small board solution size.

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[2] http://www.diasemi.com
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