Novel zero-voltage switching topology enhances buck regulator's performance

Chris R. Swartz, Vicor Corporation, www.vicorpower.com

DC-DC buck regulators are being continually challenged to provide higher efficiency and power density. While the benefit of an improvement in efficiency from, say, 88 percent to 92 percent may seem fairly modest —after all, it is only a 4.5 percent gain over the original number — that's actually a narrow view on what is driving the situation.

Certainly, higher efficiency is environmentally "friendly" and reduces the obvious operating costs for input-line AC power, as well as overall system-cooling requirements. But from a design perspective, increased efficiency has other virtues. Look at it, instead, as a decrease in loss from 12 percent to 8 percent — a significant reduction of one-third.

This improvement translates into potentially higher power densities and smaller size, along with reduced thermal management issues (heat sinks, air flow, and ambient temperature requirements) and lower operating temperatures. The result is less stress and longer life for the regulator itself as well as nearby components.

To improve efficiency, designers must focus on both power transmission and power conversion performance. Higher-voltage operation is key to efficiency, since it reduces I2R loss. In addition, by using a one-stage down conversion chain instead of two stages (i.e. 36 V to 1 V, rather than 36 V to 12 V, then 12 V to 1 V), you can reduce overall loss.

To achieve the efficiency and density improvements, the non-isolated point of load (PoL) DC-DC buck regulator must operate from a higher input voltage (larger Vin/Vout ratio), over a wider range of input voltages, while switching at higher frequencies. However, the conventional buck-regulator topology is challenged in achieving the wider input-range objective, and incurs increasing internal losses as the frequency increases.

Designers have used a variety of control topologies and techniques to overcome these issues, including current-mode control, digital control, synchronous rectification, and adaptive drivers, all supported by enhanced device packaging, higher levels of integration, and various MOSFET improvements such as reduced on-resistance. However, these innovations are reaching the point of diminishing returns when compared with effort.

Three basic problems arise as you simply try to increase the frequency of the conventional buck topology (Figure 1):

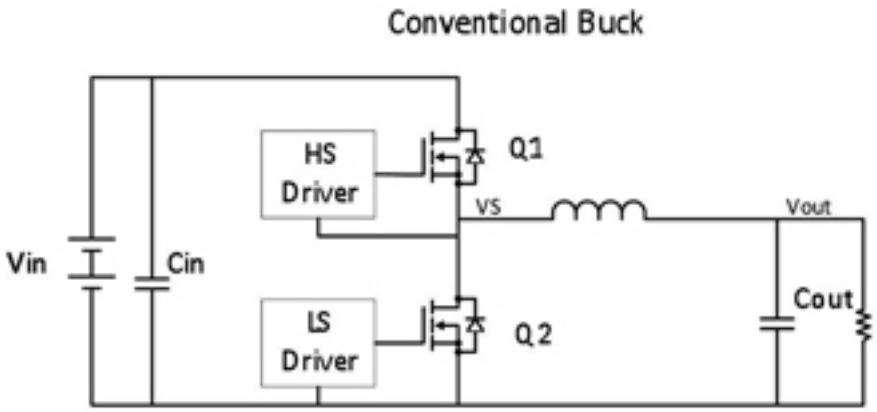

Figure 1. The conventional buck-regulator topology is long established, but is reaching improvement limitations.

•Hard-switching loss: Most non-isolated buck regulator topologies have high switching losses due to simultaneous high-current and high-voltage stress imposed on the MOSFET at the turn-on and turn-off transitions. These losses increase with switching frequency and input voltage, and limit maximum frequency operation, efficiency, and power density.

•Gate-drive loss: the gate drivers of the MOSFETs have increased losses at the higher switching frequencies.

•Body-diode loss: High pulsating currents flow through the body diode of the low-side MOSFET as the high-side MOSFET gets turned on and off. The longer the body

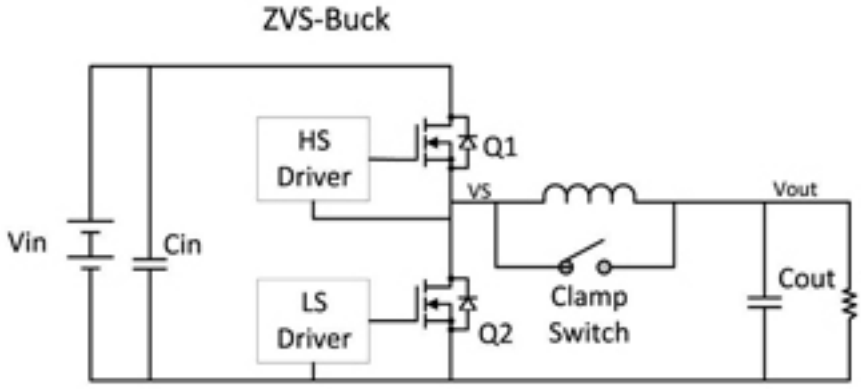

Figure 2. The ZVS approach adds a clamp across the output inductor, which offers many operating benefits.

diode conducts, the higher the reverse-recovery losses and body-diode conduction losses. This conduction causes disruptive overshoot and ringing.

In addition, the topology requires a relatively large output inductor, which adds to cost and size.

A different topology approach

For the buck regulator to operate efficiently at higher switching frequencies, the turn-on losses of the high-side MOSFET must be significantly reduced. One switching topology, however, is similar to the conventional buck regulator, but adds a clamp switch across the output inductor, Figure 2. This apparently modest

addition allows the energy stored in that inductor to be used as part of the switching cycle and reduces the turn-on losses. Note that the inductor is smaller in this approach.

Vicor’s Zero Voltage Switching (ZVS) topology is shown in Figure 2. When MOSFET Q1 is on, energy is stored in the output inductor and charge is supplied to the output capacitor. When Q1 turns off and Q2 turns on, the energy stored in the output inductor is delivered to the output capacitor and load. Q2 is kept on long enough so that some energy from the output capacitor is stored in that inductor.

When there is enough energy stored there, the MOSFET turns off and the clamp switch turns on, isolating the inductor from the output and input while at the same time circulating the stored energy, nearly without loss, as current. During this very short cycle, the output capacitor supplies the output load. When the clamp phase ends, the clamp switch opens and the stored energy is used to drive the discharging of Q1's output capacitance and charging of Q2's output capacitance.

The annotated timing diagram, Figure 3, shows the operational sequence:

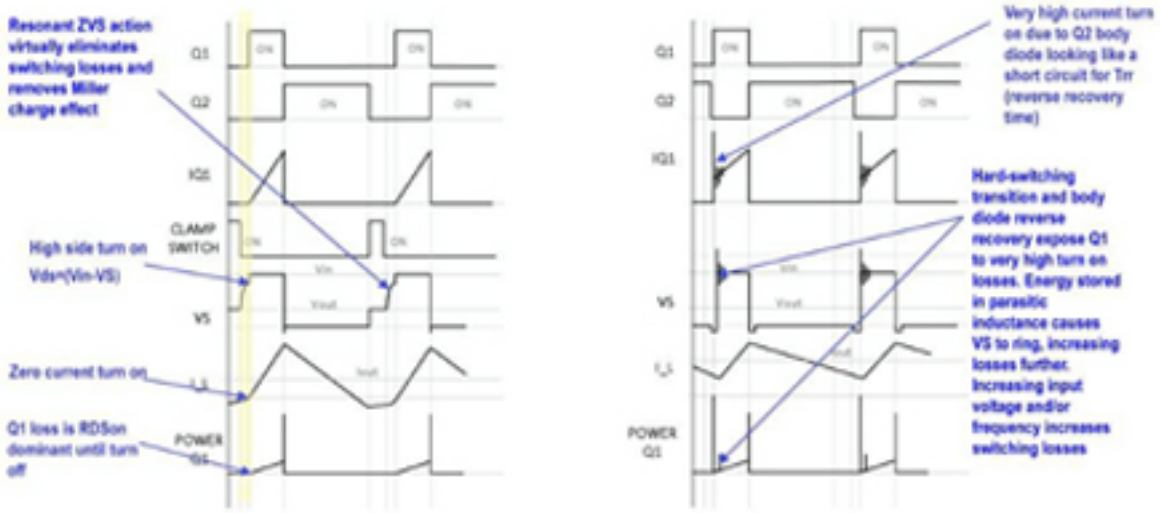

Figure 3. Operational sequence comparison of a ZVS buck versus a conventional buck.

As a result, zero voltage switching operation offers low switching losses, even at high frequencies. Additional benefits include negligible body-diode conduction time due to near-ideal rectifier switching; high-frequency operation even at high input voltage; simple internal compensation enabling high bandwidth, gain and phase margins; consistently fast transient response with a small amount of output capacitance due to small output inductor; high switching frequency, and high-bandwidth feedback loop; 20-ns minimum on-time which supports very-high conversion ratios (36:1); and exceptional light-load efficiency due to high-efficiency biasing system, combined with pulse skipping.

Figure 4. Wide input range DC/DC converter ICs implementing the ZVS buck topology.

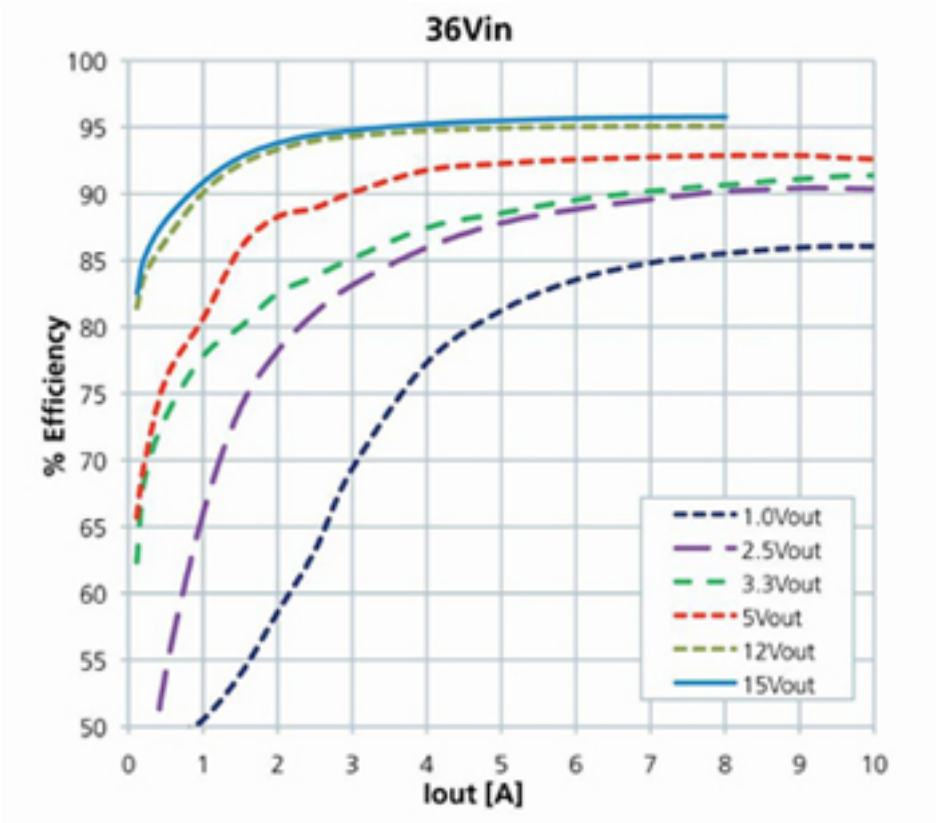

Figure 4. Efficiency characteristics of a PI33XX operating from a 36-V input for six common output voltages.

Does it really work?
The addition of the clamp switch and the associated zero voltage switching approach is not just a proposed design with benefits demonstrated solely by simulation. The PI33XX family of wide-input-range DC-DC converter ICs from Vicor implements the ZVS buck topology. These 10-mm × 14-mm SiP buck regulators require only a tiny output inductor and a few ceramic capacitors, for a total footprint of 25 mm × 21.5 mm.

Members of this product family can operate from a wide range of inputs spanning 8V to 36 V, and can deliver up to 120 W or 18 A at peak efficiency of 98 percent. At a high, efficient step-down ratio of 36 V input to 1-V output, a PI33XX can deliver 10A with 86 percent efficiency. Figure 5 shows the efficiency of a PI33XX operating from a 36-V input, for six common output voltages.

The ZVS technology is inherently stable, with a transfer-function gain slope of −1 and phase shift of 90°, which allows very wide bandwidth in the feedback loop. The high closed-loop gain and small-value output inductor mean that the output impedance is low over a wide frequency range for fast transient response, with recovery times in the range of 20 µsec to 30 µsec. The benefits of the ZVS approach have been verified and are available.

About the author

Chris R. Swartz is a Principal Engineer for Picor semiconductor solutions at Vicor Corporation. hAn IEEE member, Chris has 25 years of experience in power design engineering.