Accelerating PCB Power Delivery Network Design and Analysis

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Current design trends have made the power delivery network (PDN) of a printed circuit board (PCB) as critical as multi-gigabit data channels. Continuous increases in clock frequencies have coupled with large increases in power, while voltage levels have trended lower and lower. To make matters worse, integrated circuits (ICs) typically have multiple power domains that are unique to the device, making split planes the norm. Consumer electronics products need to perform to high standards, which include long battery life, but products must also remain cost effective.

All of these factors combine to make PDN design and analysis more difficult than ever. The very nature of a PDN—a complex system encompassing chip-, package-, and board-level domains—makes it challenging to analyze due to the differences in scale, the breadth of design choices, and the combination of analysis techniques required. As a result, power integrity (PI) analysis is now as important to the PCB design flow as signal integrity (SI) analysis. What’s needed is a comprehensive pre- and post-layout PDN methodology based on solid, accurate analysis and tight integration with the PCB design environment.

SI analysis was traditionally a post-layout verification process performed by experts. As speeds and complexity increased, more problems were found during verification that required design changes. These design changes would cause more problems, leading to an extended edit, analyze, re-edit, and re-analyze loop. Eventually this methodology proved ineffective as the number of nets requiring analysis

dramatically increased. It was replaced with a more effective methodology where upfront pre-layout analysis feeding a constraint-driven design process reduced post-layout verification problems and increased the chance of first pass success. This methodology also reduced the effort required by overburdened SI engineers, as SI became a more mainstream engineering task.

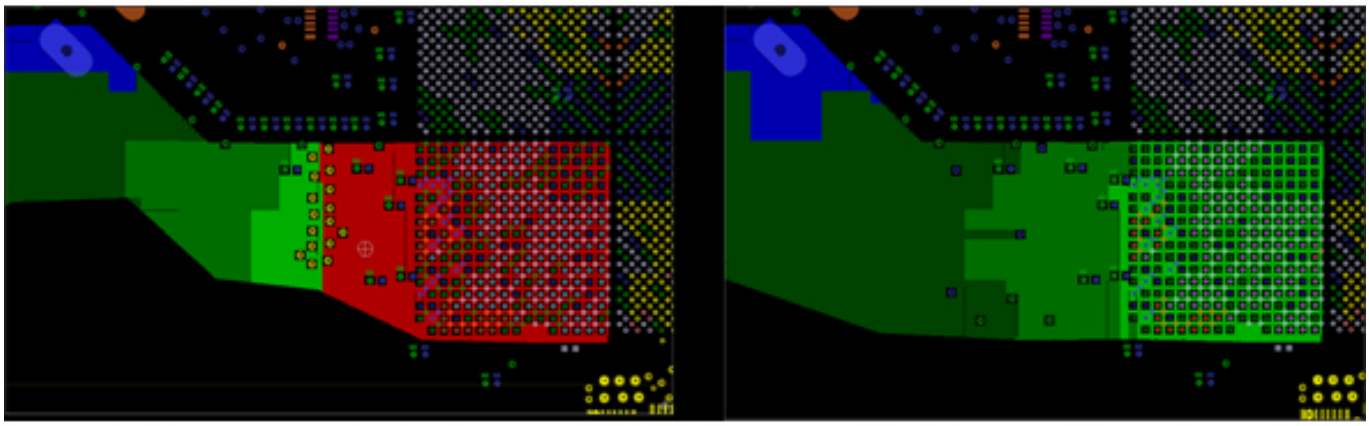

Figure 1: The picture on the left shows an area with an IR drop problem due to a via field and insufficient copper. The types of changes required are well suited to the PCB designer. If the reporting and editing are within the same canvas, the process of analyzing, editing, and re-analyzing can be very efficient.

For the better part of the last decade, PDN analysis has been the same post-route, expert-only process that SI used to be. With design trends making PDN design and analysis critical to product success, the PDN expert is struggling to keep up with demands of in-depth analysis and tight design schedules. Design teams would benefit from an integrated, comprehensive PDN analysis environment that can be used reliably by mainstream engineers.

This environment needs the right balance of accuracy and performance, and must include both DC and frequency domain analysis capabilities. In the DC domain, IR drop analysis quickly identifies problem areas on a PCB (where the layout will not provide sufficient current to the components) or potential over-design (where costly layers can be reduced). Frequency domain analysis requires the ability to detect potentially damaging voltage ripple, and the ability to maintain a desired target impedance over a wide frequency range. This analysis must span the entire PDN to allow designers to select the right number and type of decoupling caps, and to prevent costly over-design or under-design of power planes. An integrated layout and analysis environment with expert approved technology such as hybrid transmission line method and full-wave method of moments (MoM) field solvers can trade off time for accuracy, allowing for early what-if analysis and a detailed verification step that can be accessed by a larger segment of the design team as a final check.

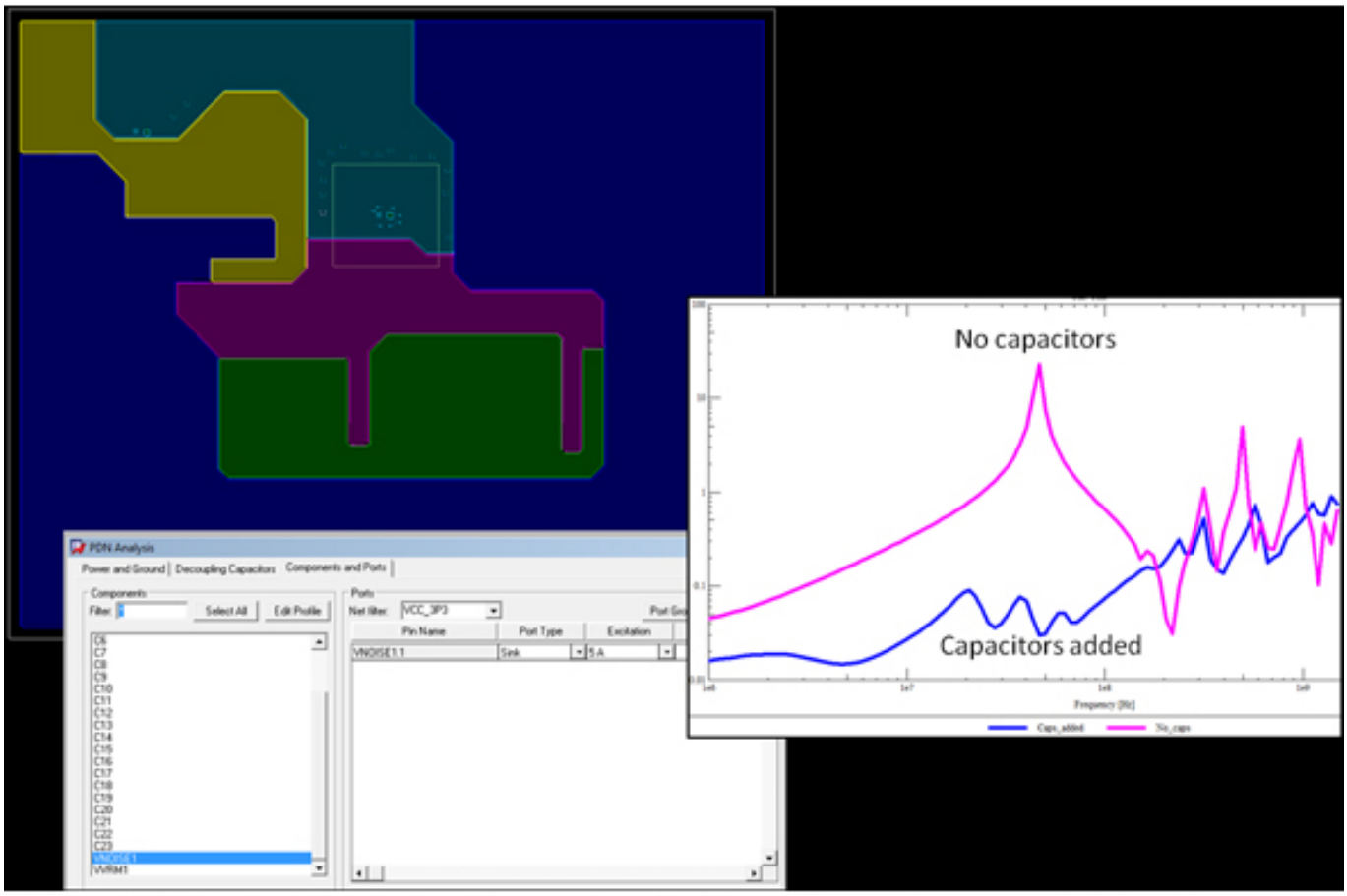

Figure 2: Early what-if analysis verifies capacitor selection, stackup, and plane splits. This can happen prior to a full netlist and should allow seamless transfer of design intent downstream.

In an integrated full-flow PDN analysis methodology, experts can be called in when a problem is found, but more of the design team can perform the analysis and efficiently address design changes. PCB design engineers are well suited to resolving IR drop problems since the required design changes are within their domain. Cleaning up a via field or adding more copper fill to a DC net within the same environment that the analysis was run is much easier than communicating required changes.

A quick re-analysis assures that the changes are correct and saves time. Moving any analysis earlier in the design cycle prevents problems from being designed-in, and integration with the design environment makes the analysis more efficient. What-if analysis can be done by varying the design stackup, decoupling capacitors, and voltage regulator modules (VRMs). When an optimal combination is found, the solution is easily committed to the design database.

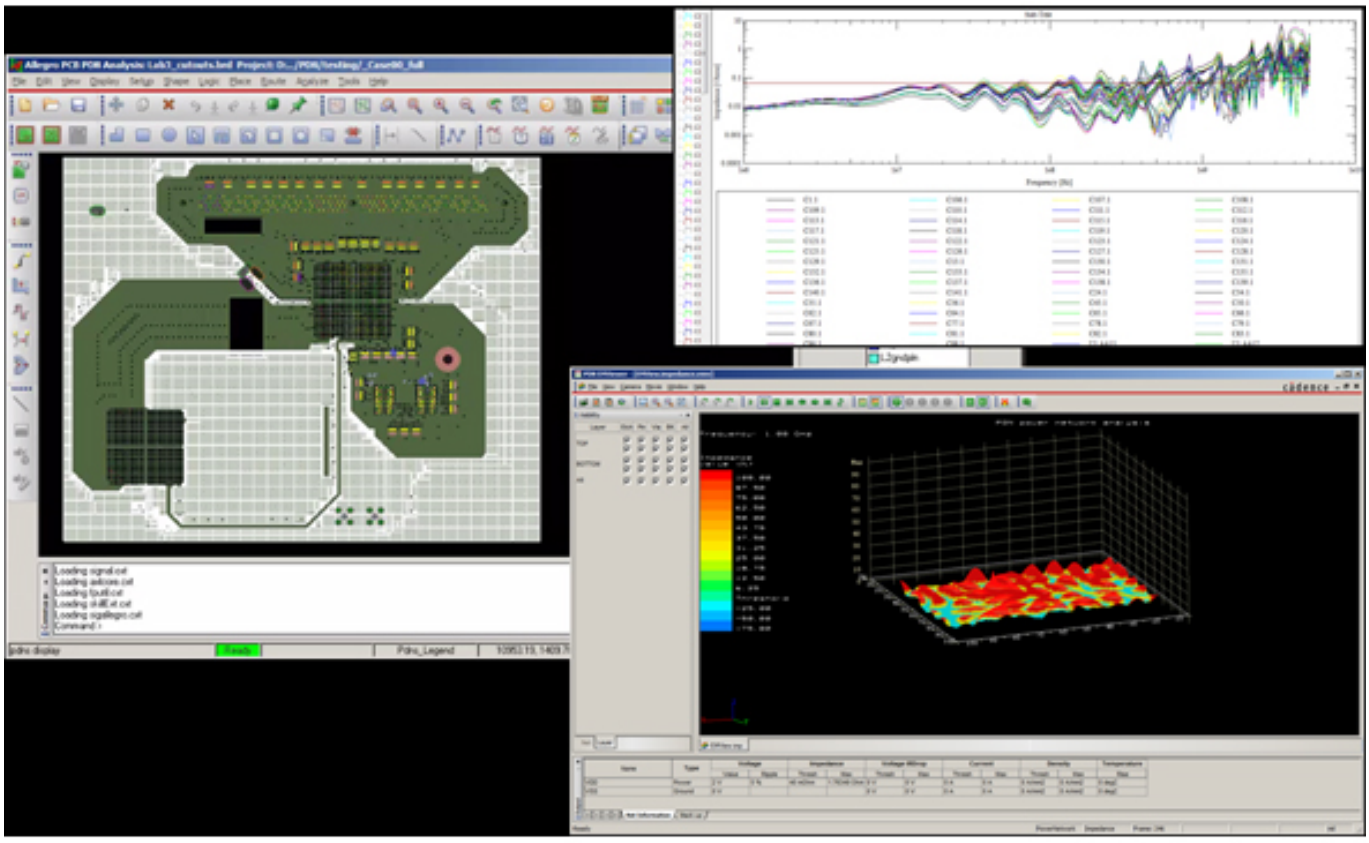

Figure 3: Post-layout PI analysis is no longer a starting point but becomes more of a final verification step once the design is completed.

Accurate and correlated PDN analysis technology can be efficiently merged with your design environment. Whether you're just getting to the realization that your current analysis routine isn't cutting it or that PDN is looming on the horizon, implementing the full layout methodology as described above can simultaneously save PCB design cycle time and cost. PDN analysis for PCBs is no longer a post-layout validation process requiring an expert. It can be applied throughout the design process to find and address PDN issues in a timely manner and ensure first-pass success.

Cadence Design Systems provides a comprehensive power delivery network analysis capability with its Allegro family of PCB design tools. It's part of a larger emphasis on low power design that encompasses chips, packages and boards, helping designers create the next generation of power-efficient electronic products.