

Multicore DSPs Power Next-generation Industrial Inspection Systems

Mukesh Kumar, Texas Instruments, www.ti.com

Advancements in both sensor/scanning and compute technologies are enabling the next generation of high performance industrial inspection systems such as post production quality assurance, metrology, robotic vision and positioning in a variety of industries from food processing, pharmaceuticals and semiconductors manufacturing. With the advent of new generations of digital signal processors (DSPs), specifically multicore DSPs, developers have high performance, low-cost and power efficient alternatives for implementing the real time image processing in inspection applications.

Today, industrial inspections systems are requiring more and more processing power due to a variety of reasons. The primary reason for needing more processing power is the fact that a modern inspection system operates on a much larger image data set and performs much more complex algorithms in real time. It is common to see multiple high resolution (megapixel) and high frame rate (frames per second) cameras streaming in large amounts of data. For example, higher-end inspections systems use multiple cameras for acquiring complete 3-D volume data and use depth cameras to have a depth profile or stereoscopic cameras to generate a surface profile.

Inspection system vendors often differentiate their products based on features implemented in software such as proprietary algorithms. They either cannot or do not want to use hardware accelerators in System-on-Chip (SoC) solutions developed by many semiconductor manufacturers for machine vision application because they do not enable them to differentiate from their competitors in either performance or quality.

The following sections highlight the typical image processing algorithms used in an inspection system and the features in multicore DSPs which provide the required processing efficiency.

Image processing

At the heart of inspection systems are many different image processing algorithms. These algorithms can be grouped into common categories like image formation algorithms, image enhancement algorithms, morphological operations, feature extraction algorithms and feature detection algorithms.

Image enhancement involves the removal of noise, enhancement of edges and contrast using non-linear filters like median filters, bilateral filters, and histogram. Edges are enhanced using algorithms like un-sharp masking or Sobel filtering, and Canny edge detectors can be used to obtain the boundaries of the important features in images.

Morphological operations are non-linear operations which use a “structuring element” to probe an image and provide a result on how well the elemental structure fits within the image. These operations can be used to thicken or lighten edges, remove small objects within a large object, connect broken edges, eliminate small holes and fill small gaps.

Most *feature extraction and detection* procedures including edge detection, line tracing, object shape analysis, classification algorithm and template matching. Sometimes the image is transformed into a different domain such as Fourier and Wavelet before the features are extracted.

DSP as the Processing Workhorse

Both image processing and data capture subsystems benefit from the use of DSPs. Homogenous multicore DSPs provide the processing horsepower needed for these compute-intensive algorithms.

Most industrial image processing subsystems require high performance in terms of core speed (GHz), MIPS (million instructions per second), MMACs (million multiply accumulates per second) and GFLOPs (giga floating point operations per second). Multicore processors, like Texas Instruments’ (TI) TMS320C6678 provide 360 GMACs and 160 GFLOPS and bring the flexibility of using both fixed-and floating-point instructions in systems which require high dynamic range. To further improve system performance, the multicore processor offers architecture designed to eliminate on-chip data transfer bottlenecks and latencies using hardware based inter processor communication.

Multiple levels of memory caching along with the amount of available on-chip random access memory (RAM) can vastly improve system performance. Since image sizes are generally much larger than available on-chip RAM, these systems invariably have a need for large external RAMs which implies the DSPs need to have high bandwidth external memory interfaces like DDR3. Shared memory architecture allows the multiple cores in a multicore DSP to either operate on different sections of the same image in parallel or perform different processing functions on the same section of image data serially. This along with intelligent direct memory access controller shared among all cores allows data transfers across external memory, memory-mapped peripherals, and on-chip memory to occur behind computations via double buffering to improve performance.

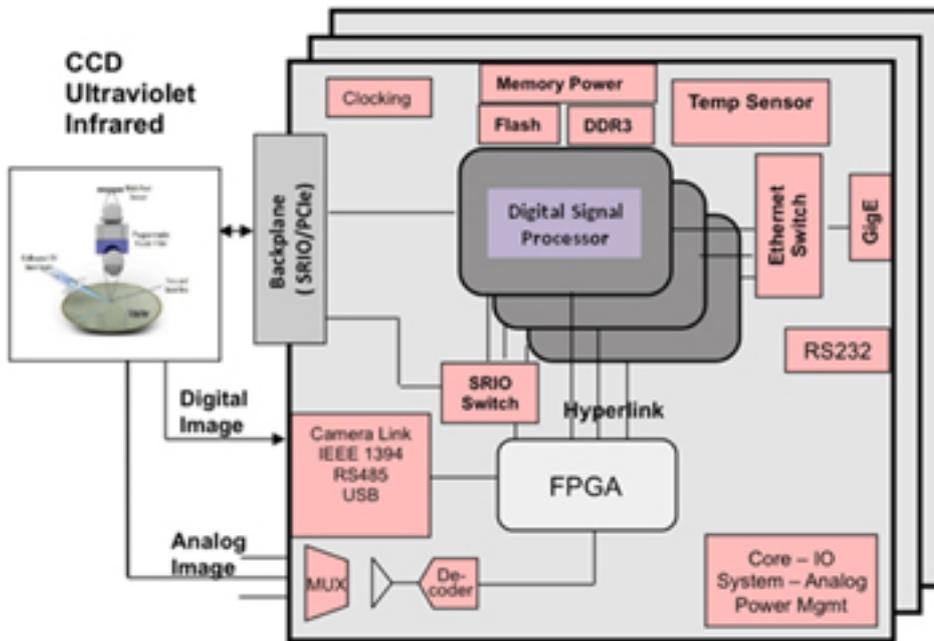


Figure 1. Industrial inspection system block diagram.

There are many options for connecting the imaging subsystem to the image processing subsystem. The system may need one or more analog or digital interfaces like CameraLink. Having a choice of high speed serdes interfaces in a DSP provides the hardware designers an option of connecting and FPGA which in turn connects with the image capture subsystem(s). TI's C6678 multicore DSP, for example, has multiple such high speed interfaces like PCIe Gen II, Serial RapidIO 2.1 (SRIO), GigE and even a 50 Gbps TI proprietary interface called Hyperlink. Sometimes the images are fed through a backplane communication fabric in which case PCIe and SRIO get used.

Since industrial inspection systems often need to be highly reliable systems capable of operating in harsh conditions using as little power as possible, multicore DSPs support extended industrial temperature grades allowing system designers to design such systems. Figure 1 depicts what a multicore DSP based image processing subsystem may look like.

For more than 10 years, multicore DSPs have shown their worth in a wide variety of applications across a range of industries. Multicore homogenous DSPs have been the appropriate choice where compute-intensive signal processing is required in a limited power budget and confined physical space. The latest generation of multicore DSPs offers exceptional computational performance, increased I/O, expanded memory, and key hardware integration that fulfill the needs of the high performance industrial inspection space. The simplicity of developing a software defined imaging system using high level language like C on DSPs accelerates the implementation of new and innovative algorithms reduces time-to-market.

About the author

Mukesh Kumar is a marketing manager in Texas Instruments' multicore digital signal processor team. Kumar received his masters in electrical engineering from

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