Probes Connect as geometries Shrink and Speeds Increase

Chris Loberg, Tektronix, www.tek.com
Before you can capture and analyze signals using an oscilloscope, you first have to connect. With trends leaning toward shrinking IC geometries, finer pitch packages and higher data rates, the connect part of the test equation has become increasingly important – and difficult – to get right. This is particularly true for miniaturized circuitry such as high-density surface mount devices where a physical connection to all the necessary test points can be challenging

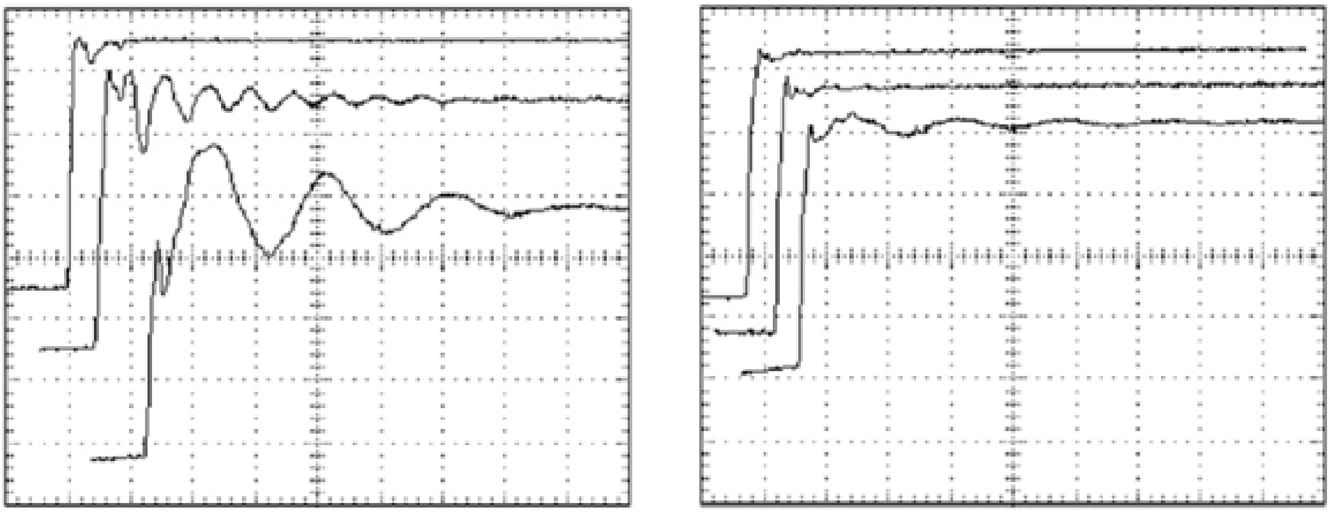
As data rates climb, measurement margin shrinks as circuit, probe and connectivity parasitics consume more as a percentage of the measurement window. This means that selecting and properly connecting the right probe for a particular application is key to attaining optimal measurement integrity using an oscilloscope.

Increasingly, engineering design teams are soldering to IC pins with 20, 16, 10 or as small as 8 mil spacing. As the solder connections become more difficult, engineers want to avoid having to move solder tips to multiple locations. It’s simply too time consuming to solder to fine pitch parts over and over again. A better approach is to use low cost leave-behind solder tips to populate the most likely points needed to validate, diagnose and debug a circuit.

The specific probing solution used often depends on where a design falls in the workflow. As a design progresses through the development lifecycle, connectivity needs change. Early on, the emphasis is on versatile signal access; later, the emphasis is more on fixtured signal access for compliance testing.

Performance Considerations
Key performance considerations for connecting a probe to a circuit include grounding, loading and dynamic range.

Any ground lead has inductance, and the longer the ground lead, the greater the inductance. When combined with probe tip and signal source capacitance, ground lead inductance forms a resonant circuit that causes ringing at certain frequencies, passive probes are particularly sensitive to this phenomenon. As the frequency of the signal increases, users should strive to reduce the length of the ground lead. It’s not uncommon to strive for ground leads of 30 mils or less for high speed serial applications. When even a short ground lead on a passive probe isn’t adequate, an active FET (Field Effect Transistor) probe can be used to minimize the ringing that is the resonance. As shown in Figure 1, FET probes, because of their high input impedance and extremely low tip capacitance, can eliminate many of the ground lead problems experienced with passive probes.



a. Passive probe. b. FET probe.

Figure 1. Examples of ground lead effects for passive probes versus active probes. Effects on the waveform of 1/2-inch, 6-inch, and 12-inch ground leads used on a passive probe (a). Same waveform acquired using the same ground leads, but with an active FET probe (b).

Loading is the process wherein a probe is applied to a test point and draws current from the test point. All scope probes load the circuit that is being tested. The key is to minimize loading to the greatest extent possible, usually by selecting the most appropriate probe for the job. Probe loading is often a result of the input capacitance of the probe. Selecting and using the right accessories can help minimize loading. Today’s active and differential probes offer excellent high DC resistance and AC impedance, which both lead to a minimal draw from the circuit.

Incorrectly using probe accessories can increase loading in some cases. Probe tip resisters in some modern probes reduce probe loading at high frequencies and help to dampen parasitic resonances caused by the interconnect between the device under test and the probe tip. Oscilloscope and probe manufacturers provide useful guides with charts and tables detailing probe loading information. These guides, or data sheets, have input impedance graphs for the various tips to indicate how much loading a probe will have at different frequencies.

One factor that is easy to forget is the position of the probe tip in the probe body relative to the circuit. For most circuits this will be negligible. But as bandwidths increase and trace impedance becomes more critical, the impact may no longer be trivial. A little forethought on how to position, attach and secure the probes will return more accurate and repeatable results. Typically, keeping the probe as perpendicular as possible to the circuit board will minimize any effect caused by probe positioning.

Dynamic range refers to the peak to peak amplitude that the probe is designed to measure with acceptable linearity. Trying to measure signals outside the dynamic range of the probe may lead to incorrect or distorted measurements and possibly damage the probe. To avoid personal safety hazards, as well as potential damage to the probe, it’s wise to be aware of the voltages being measured and the voltage limits of the probes being used.

One of the more significant advances in probes of late is the introduction of TriMode probes. With these probe tips, a single probe setup attached to an oscilloscope can make differential, single-ended, and common mode measurements without moving the probe from its connection points. Improved productivity is achieved by reducing setup time. One setup can be used to make the three different types of measurements all with the press of a button.

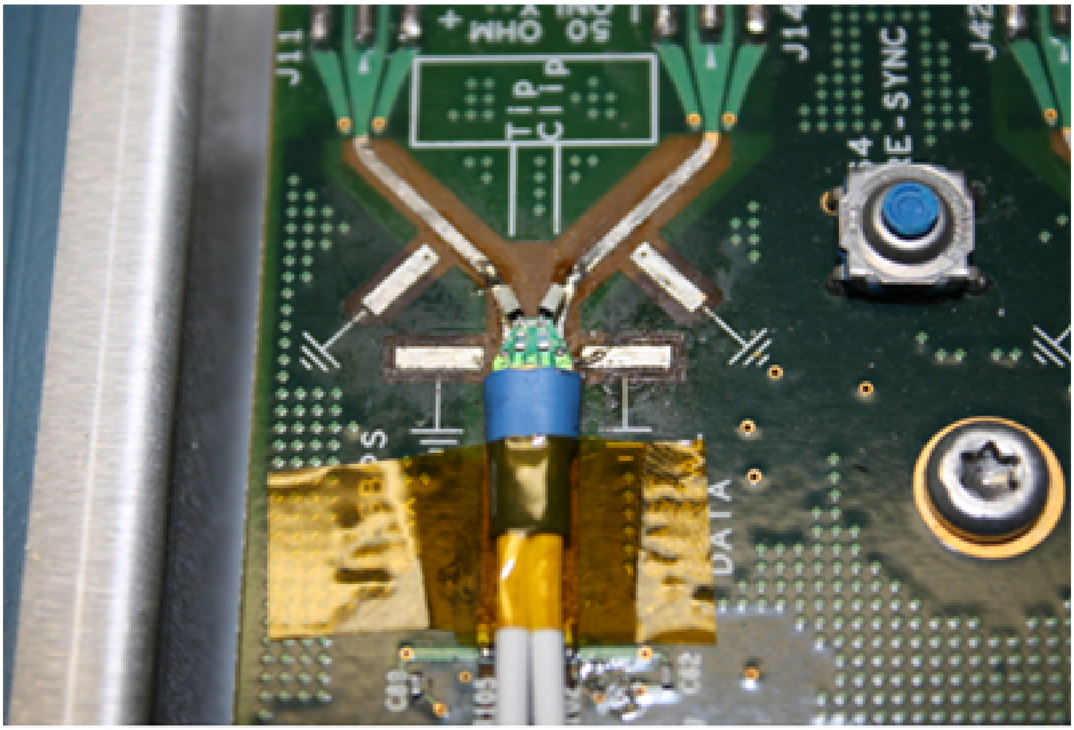


Figure 2. High speed TriMode probe tip set up to make differential, single-ended, and common mode measurements with one connection, also illustrating the probe tip resistors that minimize the parasitic resonances. For delicate measurements, secure the probe tip.

Testing DDR DIMM signals is a common challenge in the surface mount space. In particular, connecting probes to DIMM modules is one of the main difficulties for testing DDR, DDR 2, and DDR 3 DIMMs. Signals on the DDR DIMM module may be hard to access, especially when two or more DIMM modules are inserted adjacent to each other. With 20 or more test points on a board that need to be tested (Figure 2), probes need to be easily and reliably moved from point to point without having to turn off the DUT. With so many test points on a DIMM and each needing its own solder tip, cost can quickly become an issue. Vendors may need to test dozens, if not hundreds of DIMM modules a year, so the tips need to either be inexpensive or easily reusable.

Figure 3. Example of a quick connect micro-coax solder tip.

One approach to solving this problem is a micro-coax tip that consists of a square pin connector and a small circuit board with axial-leaded resistors separated by over an inch of micro-coax cables. The axial-leaded resistors are ideal for soldering to small circuit board features. The micro-coax is long enough that connections to the socket cable can occur at the top of a DIMM and also act as strain relief for the solder joints.

For compliance testing and other applications, a low-profile interposer can minimize probe-induced effects on the DDR3 bus. An interposer probe is inserted into the target memory socket while also accepting a memory module in the probe's extender DIMM slot. This capability is essential when the target system has only one memory slot, or when a user must probe a fully-populated memory bus.

Summary

Every device and its associated probing requirements are different. That’s why manufacturers offer dozens of different probing and accessory combinations. In this case, the manufacturer’s representative is a critical ally in helping you find the probes and accessories that are both cost efficient and signal friendly. And don’t forget to keep lead lengths as short as possible.