# Prototyping with Frequency-Flexible Crystal Oscillators

Phil Callahan, Sr. Marketing Manager, Timing Products, Silicon Labs

Developers of new systems ideally should make decisions regarding clocking requirements early in the design process. Although clocking rates are critical parameters that should be known in advance, determining these rates sometimes requires experimentation and re-evaluation. The ability to quickly change clock frequencies during the prototyping and validation stages of a design can accelerate time to market. The use of frequency-flexible, programmable crystal oscillators (XOs) as prototyping tools can facilitate the process of validating system performance and help streamline the overall product development cycle.

**Evaluating Multiple Frequencies**
When conducting any system design effort, frequency changes often become necessary late in the design cycle. For example, experimenting with and optimizing clocking rates during the development process often leads to improved performance and a more efficient design. In other cases, a bug or miscalculation in the design may require a change in frequency. In any of these situations, it helps to use XOs that are adaptable to last-minute changes without having to change the bill of materials or PCB layout, especially since lead time for fixed-frequency XOs may extend the development by weeks or even months.

Last-minute changes are very common, especially in FPGA-based applications. The extreme flexibility of FPGAs means that logic path widths and data rates can be quickly adapted to improve power, throughput or gate utilization. For example, changing data path width or decreasing the clock rate may be an effective way to close timing in the final stages of an FPGA design. In addition, there may be mixed-signal circuits, such as on-chip serializer/deserializer (SerDes) transceivers, that may benefit from clocking optimization. Output jitter performance and bit error rates often depend directly on the reference clock frequency. The ability to quickly change clock frequencies helps arrive at the optimal clock rate.

**Frequency Margining**
Systems that use standard frequencies can also benefit from frequency-flexible XOs for design validation and frequency margining during production test. Although an Ethernet MAC or PHY may specify a 156.25 MHz reference XO, a fixed-frequency reference cannot exercise rate tolerances. To margin the system, designers must use external clock sources that can generate 156.25+100 ppm and 156.25-100 ppm MHz, or they must rework the board to install faster or slower XOs. This method becomes limiting and time-consuming, especially when multiple boards are being tested across many temperature conditions.

Frequency margining also can be carried out using multiple XOs and a multiplexer as shown in Figure 1. The disadvantages of this scheme include the limited number

of frequencies and the introduction of additional noise and phase discontinuities that occur when switching between frequencies. This approach also requires a different PCB footprint for validation and production.

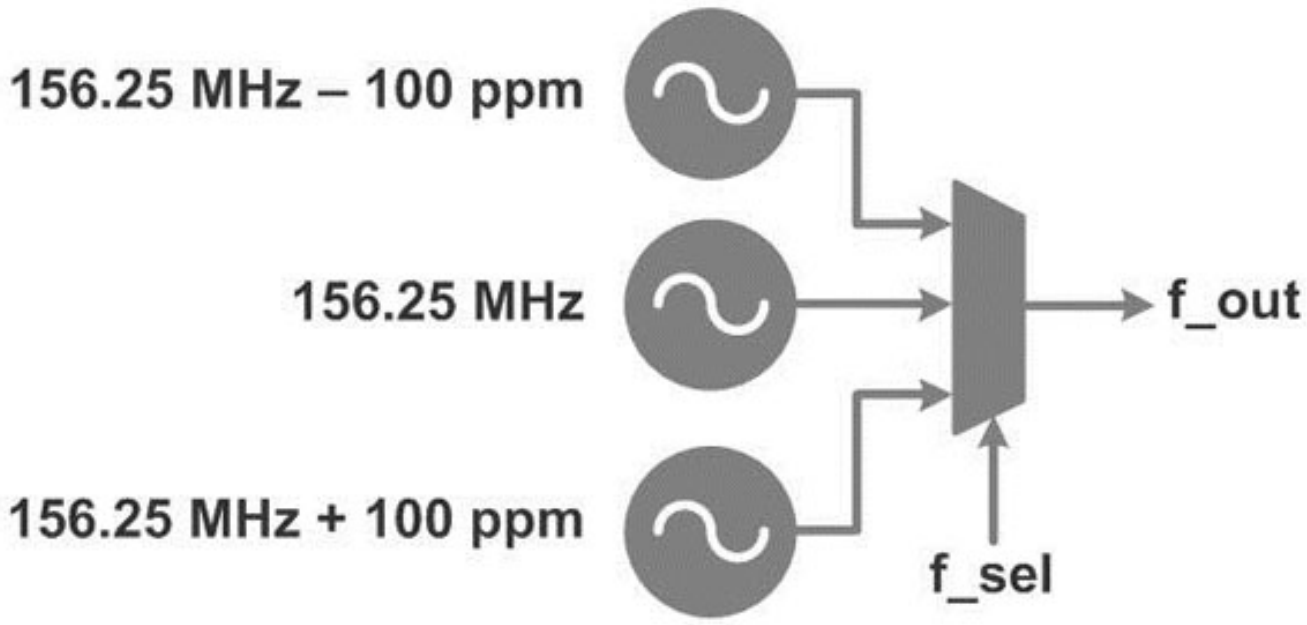


**Figure 1. Frequency Margining Using Multiple XOs and a Multiplexer**

Using external clock sources or multiple XOs to perform frequency margining often limits the designer's ability to make fine frequency adjustments or validate a continuum of frequencies to troubleshoot suspected problem areas. This issue may result in added re-work and increased delays due to the lead time needed to obtain additional clock frequencies. For example, if the system works at +100 ppm but fails at +55 ppm, neither of these approaches will catch that failure effectively.

**Traditional Frequency Flexible XOs Do Not Meet the Challenge**

A better approach to the problem of performing frequency margining is to use in-circuit programmable XOs that can generate a continuum of frequencies with very high incremental frequency resolution without introducing phase glitching or compromising phase jitter performance. Traditional XOs cannot accomplish this frequency flexibility because they rely on mechanically tuned quartz crystals that are cut to resonate at a particular frequency. Each new frequency requires a different crystal dimension.

To address this need, traditional XO suppliers use analog circuit techniques such as phase locked loops (PLLs) to overcome the frequency rigidity of conventional crystal oscillators. However, analog PLLs are often limited to powers-of-two or integer frequency multiplication. These solutions cannot meet the frequency resolution required to provide the designer with total frequency programming or "tuning" flexibility.

**Power Supply Rejection Performance Also Affects System Prototyping and**

**Debug Time**

Analog PLLs are notoriously sensitive to noise, often coupling and amplifying noise sources through the power supply and internal VCO to the output clock signal. This sensitivity prevents analog PLLs from driving ultra-low jitter clock signals in high-performance systems where clocking flexibility is important and the environment tends to be noisy and hostile. To address all of this power supply noise, PCBs must often be modified or redesigned during the time-critical prototype debug phase, which significantly delays system validation and eventual production release.

The system noise is largely due to transient load switching currents and the widespread use of switch mode power supplies (SMPS) in most computer, communications and consumer systems. To combat the noise and ripple generated from these SMPSs, integrated on-chip supply voltage regulation and filtering is becoming a necessary feature not only for fixed XOs, but for programmable XOs as well. Integrated regulation and filtering helps reject the noise that is common on the power supply rails so that it does not compromise the jitter performance of the output clock. In most cases, the extra PSR performance will improve jitter margin, extend link range and enhance system performance compared to traditional analog-based XOs.

Integrated filtering and regulation translates directly into a BOM cost and component count savings since designers can minimize or even eliminate external power supply filters and ferrite bead components needed to maintain adequate jitter performance. For example, assume a 100 mVpp sinusoidal ripple over a range of 100 kHz to 1 MHz is present on the power supply of an analog PLL-based XO. Switching power supplies necessary to improve system power efficiency commonly operate over this frequency range. Noise of this magnitude on the power supply can degrade the jitter performance of typical XOs using an analog-based PLL without on-chip filtering and regulation from approximately 10 ps (without supply noise) to over 50 ps (with supply noise). This reduced jitter performance makes common analog PLL-based XOs unsuitable for high speed networking applications, such as Gigabit (GbE) and 10 Gigabit Ethernet (10GbE).

The bottom line? The performance and frequency limitations of analog PLL-based XOs force system designers to use fixed-frequency devices that often lack integrated supply regulation and filtering. As a result, designers find themselves back at square one with very few options.

**I2C Digitally-Programmable XOs Offer a Versatile Solution**

I2C digitally-programmable XOs provide a flexible alternative to fixed-frequency XOs. For example, as shown in Figure 2, Silicon Labs’ programmable oscillators combine a traditional fixed-frequency crystal reference and patented DSPLL technology to provide an I2C programmable output with adjustable frequency resolution better than 26 parts per trillion. Because of their unique digital circuitry and extensive internal power supply regulation filtering, oscillators based on DSPLL technology easily achieve jitter performance comparable to fixed frequency SAW-based oscillators. I2C programmable oscillators enable the evaluation of any frequency in a system without sacrificing performance. Moreover, I2C-programmable XOs can be ordered with a default start-up frequency, and they are

pin- and performance-compatible with fixed-frequency XOs.

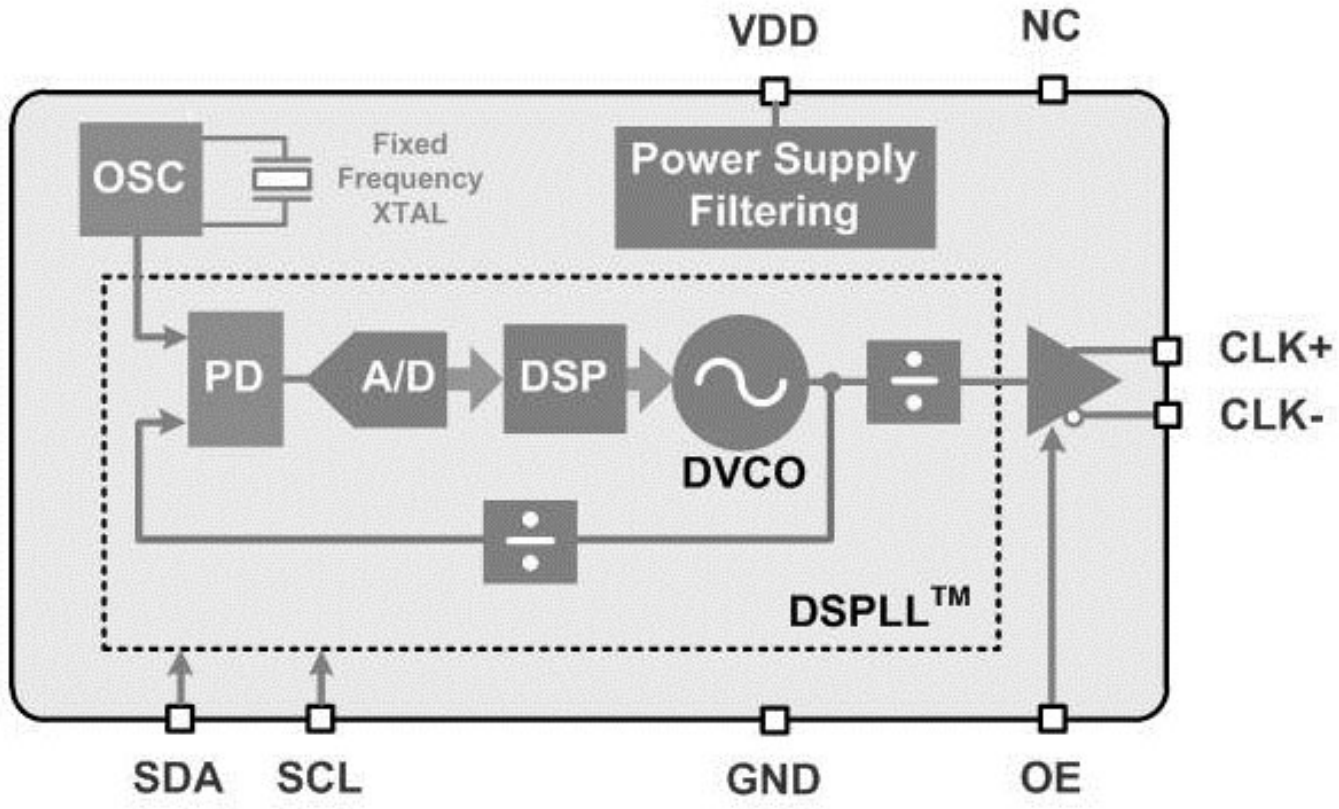


**Figure 2. Example of Silicon Laboratories' I2C Programmable XO Architecture**

By using frequency-flexible, I2C-programmable XOs as prototyping tools, developers can greatly simplify the process of validating and maximizing system performance while streamlining the overall product development cycle. The ability to change clock frequencies without changing the bill of materials, reworking the board design or waiting for long-lead-time XOs can help the designer reach business-critical time-to-market goals while optimizing features and performance.

**Source URL (retrieved on *08/31/2014 - 12:58am*):**
http://www.ecnmag.com/articles/2011/06/prototyping-frequency-flexible-crystal-oscillators