Addressing Product Miniaturization Challenges for Medical Electronics

Vern Solberg, Tessera Technologies

With the rapid deployment of new products from an ever growing number of competing companies, time-to-market can be the difference between leading and following. For that reason, many manufacturers will rely heavily on more innovative package solutions that minimize overall package size as well as integrate a number of already proven functional elements within a single-package outline. The challenge the medical electronic developer faces when competing in this very specialized field is to offer a product that will meet all performance and functionality expectations in a form factor that is significantly smaller and lighter than the product it’s replacing. Simultaneously, the newer generations of electronic assemblies are expected to exhibit a higher level of reliability and long service life. The medical electronic industry has traditionally relied on two options for adapting active silicon die functions; commercial plastic encapsulated devices or the uncased bare die. The commercial package has the advantage of being fully tested before board level assembly but its somewhat bulky size limits the product designers’ ability to reach the more aggressive requirement for reducing the end product size.

A growing number of memory products are being configured in a vertical format; die-on-die or package-on-package. Although a number of memory products have evolved in the vertical format, many of the multiple-die configurations combine both memory and logic functions. Early applications employed the classic wire-bond process for die interconnect, however, other applications can utilize alternative die interface techniques, including wire-bond, and/or a combination of wire-bond and flip-chip methodology typical of that shown in Figure 1.

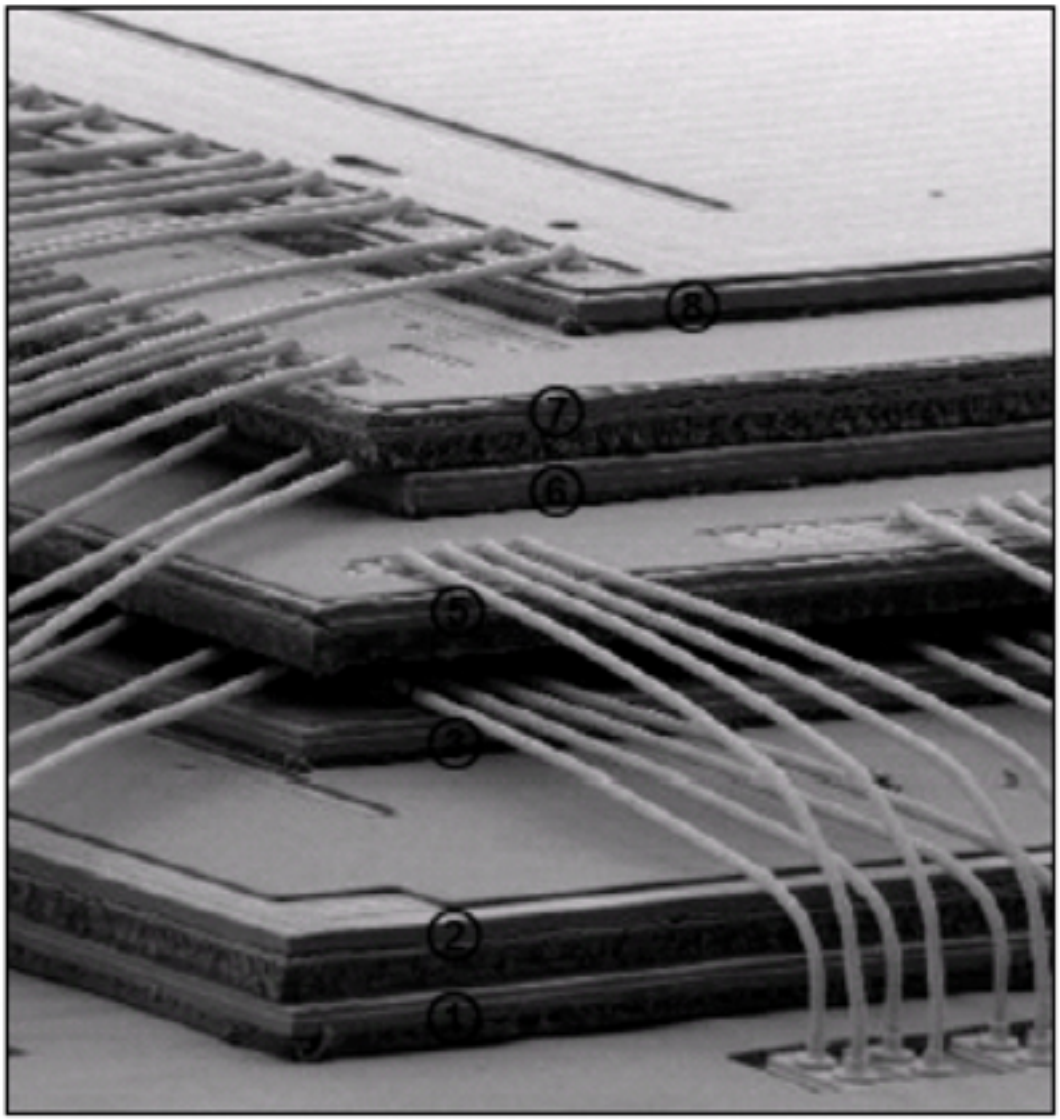

Figure 1. A custom eight die flip-chip and wire-bond assembly developed for the 3G phone market.

Increased memory capacity is a primary goal for many applications. Most of the higher performance memory products currently in the market have significantly greater lead count than their lead-frame predecessors. To better facilitate package-to-board interface most of these devices are attached to a dielectric substrate and furnished with contact features configured in an array format. One of the more mature processes for interconnecting the semiconductor and package substrate is the wire-bond. The process is primarily applied when the die is mounted ‘face-up’, away from the package substrate surface; however, because a number of memory die are configured with center located bond features, the wire-bond process can be performed with die mounted ‘face-down’ against the package substrate. To accommodate face-down wire-bond, a slot must be provided in the substrate to access the bond pads on the die. The example shown in Figure 2 is a high performance face-down memory die with center located bond pads assembled using a ’ through-slot’ wire-bond process. The package outlines furnished for most of the high performance single die memory products are only slightly larger than the die outline.

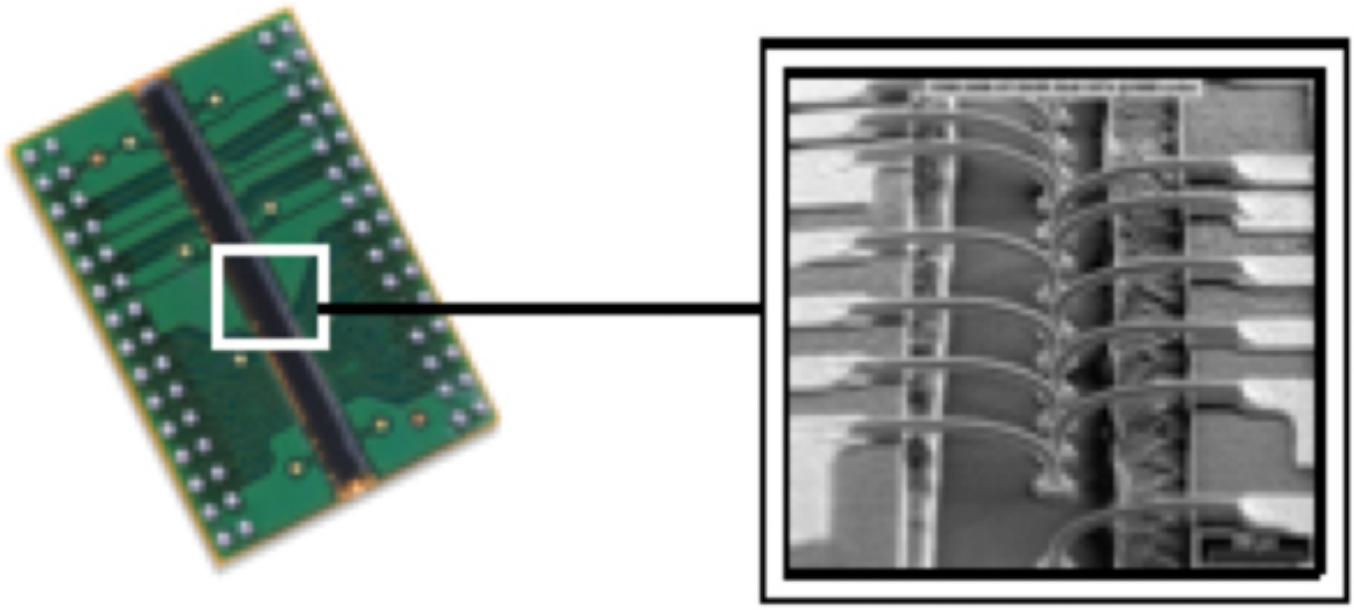

Figure 2. High performance memory using through-slot wire-bond interface between the die bond pads and the package substrate.

Vertically stacking packaged die (package-on-package) has become more attractive to many OEMs. Stacking packaged die has proved to have less risk because the packages are tested before conversion to the stacked format. Package stacking of memory products actually began with lead-frame plastic packaged ICs over a decade ago. Even then, the market needed increased memory density for modules used for computing. Although the lead-frame stacking process cost was significantly greater than the basic packaging cost of the single die component, the single module substrate enabled the doubling of memory density without impacting module size. Although the single die memory package will be supplied with all contact features within the confines of the packaged die outline but to enable stacking one package above another, the substrate is extended outward so that the contact features are outside the die outline. The example furnished in Figure 3 illustrates a straightforward vertical integration of four FBGA packaged memory devices joined together using pre-formed spherical tin-silver alloy contacts. By combining these pre-tested semiconductor packages, there are never any compromises made in testing or subsequent assembly processing. The two and four level memory package is currently experiencing the strongest market appeal but a growing number of companies are discovering that any number of functions can be combined in this format.

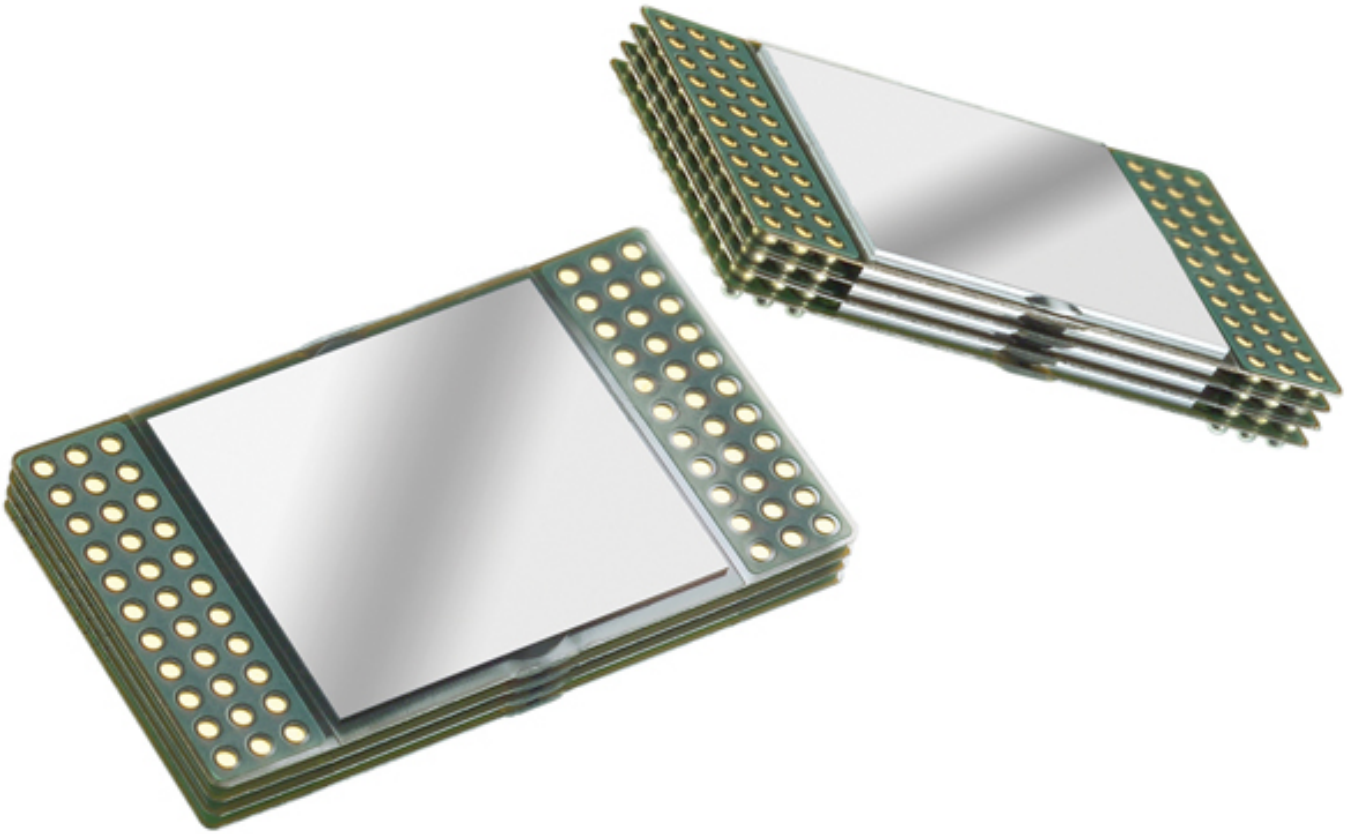

Figure 3. The vertical stacking of packaged memory enables significantly higher component density.

Medical electronic companies working on specialized, high-end applications will likely need a combination of logic and memory. Product designers have found that, although a multiple function product can be made significantly smaller by using bare, uncased die, establishing and managing multiple sources for bare die can be difficult. In addition, handling and electrically testing the uncased product requires specialized skills and capability. Additionally, bare die test methods can vary a great deal from one supplier to another and the test method applied may not meet the same criteria as that furnished for packaged die. System-in-Package (SiP) for medical applications may require more complex mixed-technology functions, and some companies may choose to combine several of these functions onto a single silicon die. The development time and costs for custom semiconductor development, however, can be excessive. Package-on-package, development using existing silicon, on the other hand, is much quicker and is far less expensive. The vertically stacked package can easily include the mixing of logic, analog and memory, e.g., baseband and flash, flash and SRAM or multiple flash-memory with a controller in a configuration typical of that shown in Figure 4. Even though test methods will vary significantly when adapting these multiple die configurations, the users can be assured that each package will be supplied as a fully tested component or subsystem that can be certified by the supplier companies before board or module level assembly.

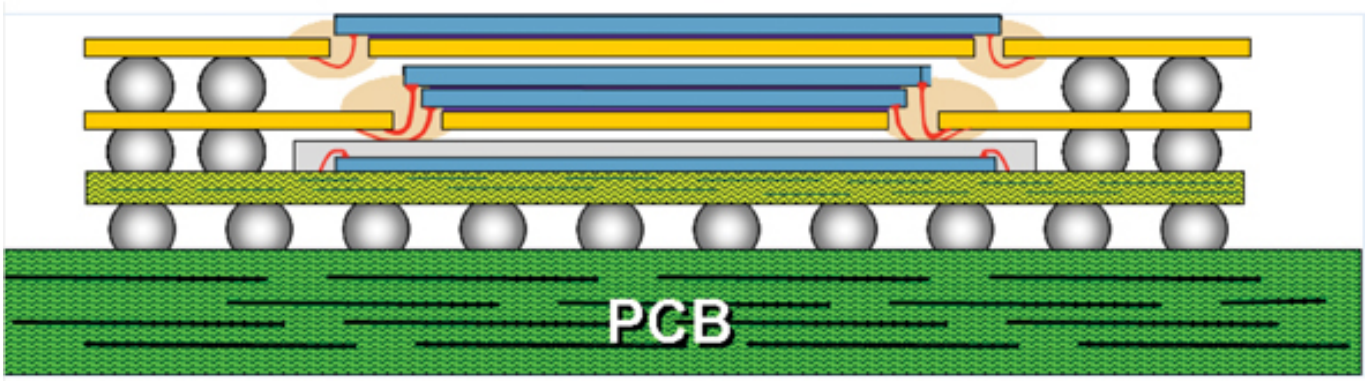

Figure 4. Package-on-package assembly can furnish higher assembly process yields by joining pre-tested mixed function devices.

The expanding functionality expectation for medical electronic products has opened up a whole new category of IC package technology. This factor has increasingly become an issue and is evidenced by the physical restriction on the number of ICs that can be designed onto the circuit board. Package performance is also an issue. Until recently, the component packaging industry did not directly concern itself about system level performance, but, as multiple die are configured into a single package outline, the whole system performance issue must be kept in view. Any comparison, however, should be done at the equivalent system level; one composed of single device packages and the other with multiple die packages and their interface methodology. As noted above, the perimeter located contact pattern of vertically stacked package is designed to allow one package to sequentially mount on the top of one another providing the interface between package layers and the eventual termination to the board or module level assembly. This, in turn, allows the overall profile height of the multiple die package to remain relatively thin.