

Meeting the Demand for Complex Communications Design

Jon Friedman, Aerospace and Defense Marketing Manager, MathWorks



Communications engineers today must design to accommodate changing missions, shorter product lifecycles, and increasing computer power. Using Model-Based Design, engineering teams developing advanced communications systems can collaborate in a common environment enabling them to capture the algorithm design as well as system-level effects of non-idealized hardware.

In the initial stages of the design process, systems designers and implementers often guess whether to use analog or digital components, and what portion of a design should be implemented in software or hardware. Typically, it is only near the end of the design process that they find out if the guess meets performance requirements. If not, significant rework may be required – leading to cost and time overruns.

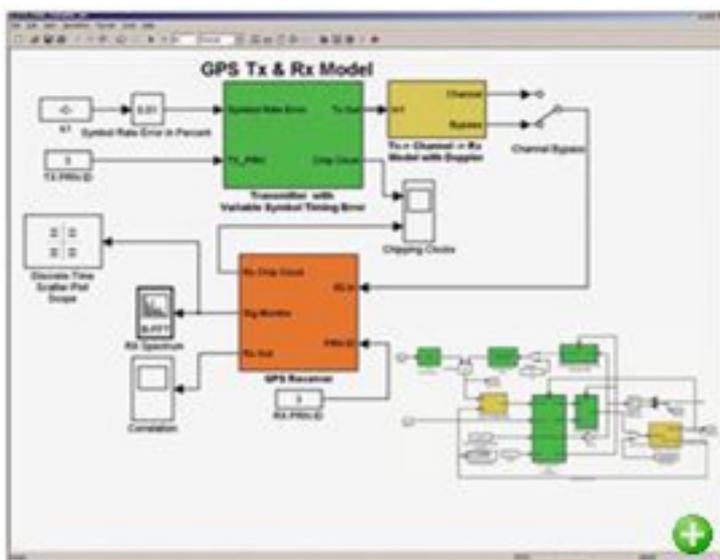


Figure 1. Top-level view of a GPS system.

With Model-Based Design, engineers create an executable model that allows them

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to develop, test, and partition the design prior to implementation and integration. This approach reveals errors early on, when they're easier and less expensive to fix.

Here is an example of how Model-Based Design could be used to develop a GPS receiver.

Design process overview:

Step 1. Start by creating a system-level model of a GPS receiver from the written specification for a GPS physical layer. The model contains the transmitter (to introduce timing errors to test the receiver timing recovery control loop); a channel (which adds Doppler shift to test the receiver carrier tracking loop); a receiver; and measurement visualization subsystems. Once the simulation meets performance goals, the system-level model becomes an executable specification.

Step 2. Partition the algorithm model into a portion that will reside in the FPGA and a portion that will reside in the floating-point DSP.

Step 3. After the receiver model is working with floating-point arithmetic, elaborate the model with fixed-point attributes that will be required for the FPGA partition.

Step 4. Automate implementation on the FPGA using the fixed-point model of the FPGA partition with tools such as Simulink HDL Coder or Xilinx System Generator. Then, using an HDL simulator, verify that the implementation is functionally equivalent to the design model. Similarly, using the model of the DSP partition, the C code can be automatically generated by tools such as Real-Time Workshop Embedded Coder for deployment. Before integrating the C onto the DSP, it can be pulled back into the simulation environment and checked against the model to confirm functional equivalence, as was done with the HDL code.

Step 5. Deploy the HDL to the FPGA and the C to the DSP. Confirm that no errors are introduced on the target hardware.

With Model-Based Design, teams can optimize their designs through design exploration, identify errors prior to implementation, and use modern commercial off-the-shelf (COTS) tools to automate much of the work.

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