

# Making OpenVPX Work for Your Mil-Aero Application

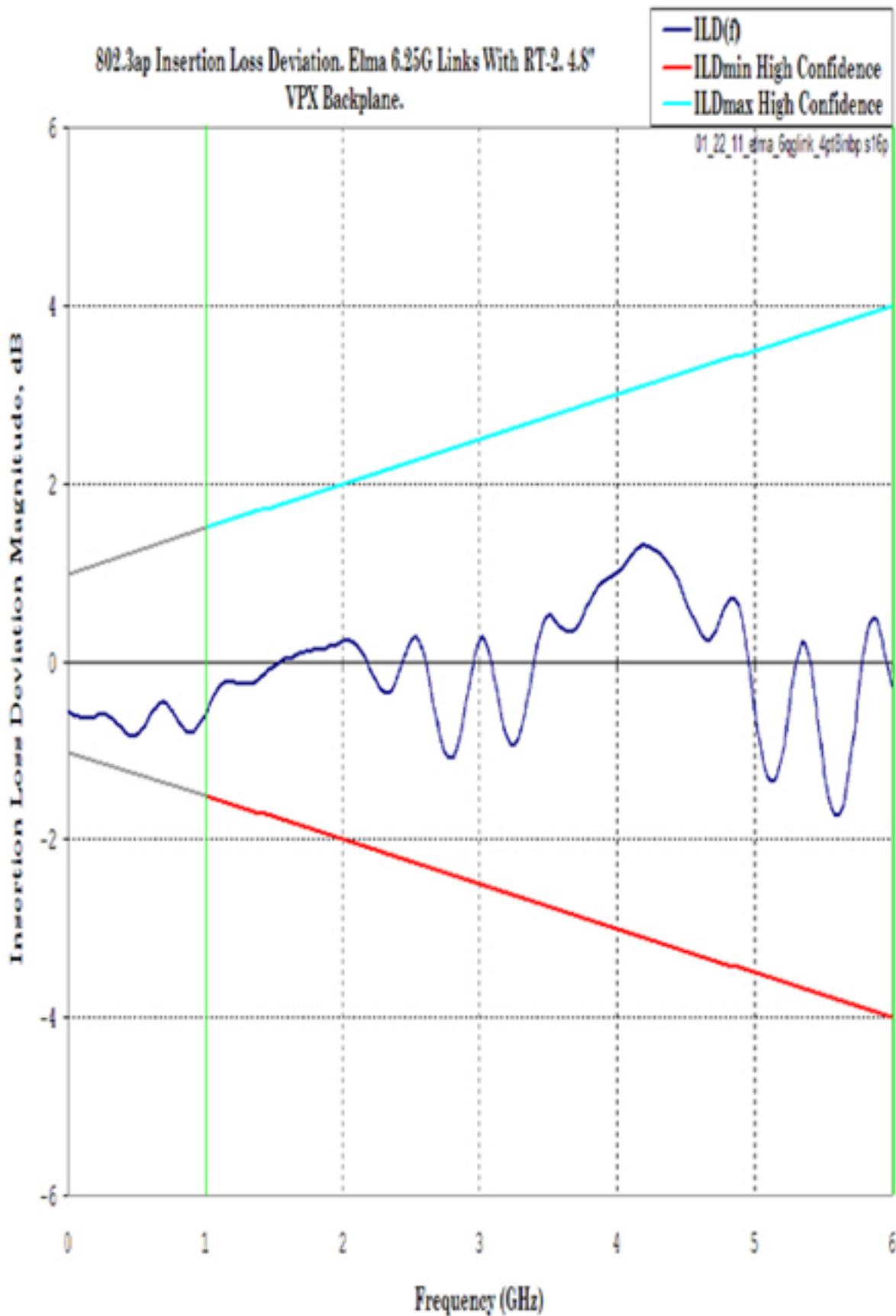
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OpenVPX is a critical new open standard architecture that has gained rapid acceptance in the Mil/Aero embedded system community. However, the VITA 65 specification for OpenVPX is very complex, and there are potential pitfalls. The primary challenges are working with the very high signal speeds of VPX, prototyping and testing to the architecture, and finding convenient IO and RTM solutions. Elma Bustronic will discuss the design challenges and potential solutions to the problems that designers are discovering today.

### Speed and Complexity

One game changer for Mil/Aero systems is the complexity of the OpenVPX architecture and the performance challenges across the backplane to meet high-speed demands. OpenVPX is an effort by the VPX community and standards bodies to provide definitions for system interoperability. VPX is a highly flexible architecture, allowing so many configurations and topology options, that it was difficult to ensure interoperability between VPX systems. OpenVPX solves this problem by defining profiles for the board modules and backplane slots. The VPX modules and slots across the backplanes have been given definitions so that similar modules will work within certain slot configurations. The backplane configurations have been defined to show the collection of slot profiles it entails, including information on the data rate, routing topology, and fabric used. Now, the integrator can determine that a daughter card module from company "A" or company "B" can be used in the same backplane slot as company "Y" or company "Z", when both module profiles specify the same slot profile.

The speeds across the OpenVPX backplane are 3.125, 5.0, or 6.250 Gbaud/s. Achieving the 5 and 6.250 Gbaud performance across the backplane while maintaining clean channel signals can be a challenge. Backplane pre-design simulation and post design characterization are now an increasingly critical part of an OpenVPX system's design (See Figure 1). This includes testing across the backplane and the full interconnect path. With the advancement of newer multi-gigabit specifications (10GBASE-KR, 40GBASE-KR4, CEI-28G-VSR, etc), and high-speed signals in architectures like VPX, performing signal integrity analysis for backplane channels becomes not only recommendable, but mandatory. Pre-layout and post-layout simulations as well as actual lab measurements, followed by studies correlating the simulations with measurements should be in the toolkit of any designer working in the multi-gig channel realm. Backplanes present unique challenges with regard to embedding/de-embedding certain portions of a backplane channel and the accuracy in performing simulations and measurements to properly compare models to test results is crucial.



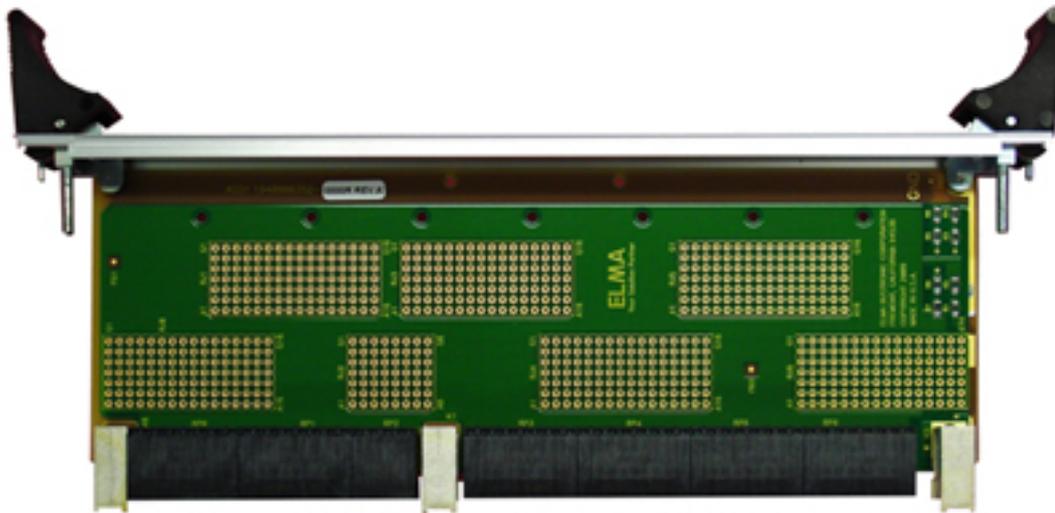
**Figure 1. The insertion loss deviation chart for a 6.25Gbaud/s VPX backplane.**

Another challenge for VPX systems is handling IO requirements without getting into

heavy customization. A dedicated RTM is one potential solution.

## RTMs & Cables

An RTM helps bring IO off the backplane in a convenient pluggable module. Injector/ejector handles help securely fix the board in place providing a more reliable connection. Direct plugging also offers better resistance to shock and vibration than ribbon cable connections. With the flexibility and wide range of configurations for VPX, RTMs for the architecture are highly customized. In some cases, a Universal VPX RTM Breakout Board can be used (Figure 2). It allows a test engineer to access I/O signals on custom-built VPX boards. The board would typically be used to bring out single-ended TTL signals that might be part of an engineer's custom IO board. Since the VPX breakout board would not be intended for high-speed signals, custom RTM boards are required in some cases. Another possible solution is the use of direct VPX Cabling.



**Figure 2. A VPX RTM breakout board allows versatile paths for single-ended signals for I/O access during prototyping/testing.**

With the design flexibility of VPX, there are many configurations available for all types of applications. But, for certain requirements for IO, out-of-band communication, etc., achieving the intended design goals could be challenging. Using custom designed RTM modules for VPX is one solution. But, for development and deployed systems, the time, costs, and complexity for certain requirements can make that solution prohibitive. The cabling system allows the designer to connect one slot to another or have connectors on one end such as RJ45, 38999 circular connectors, SMA contacts, and more.

The VPX Cabling solution from Elma Bustronic helps solve these problems. One VPX wafer comprises of four coax wire lines, so both differential pairs are terminated. Each wafer therefore consists of an ultra-thin pipe. To create a thin pipe, the engineer can simply snap together two wafers. For a fat pipe, snap together four wafers. The wafer modules plug directly into backplane slots and can be securely latched with optional locking bars. For rugged deployed applications such as Mil/Aero, ensuring that the cabling solution can withstand shock and vibration is

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critical. Therefore, locking bars are supported in a metal shell which outlines the Multi-gig connector. The shell is mounted down with screws using the same type of implementation that has been used in other rugged/military designs for decades.

### **SerDes Testing**

A VPX Cabling System can also be connected to a SerDes test device to create a simple “health monitor” for the VPX signals. This type of device allows fast and efficient BER testing for VPX backplanes, boards, or the full interconnect path. The wait queue’s for a full room of test equipment (let alone a specialized SI engineer) can be staggering. With a simple-to-use device, BER testing and pattern generation can be done with a laptop, downloadable software and a small space for the SerDes Test Unit and hardware.

### **Conclusion**

OpenVPX can be an ideal architecture for a high-performance Mil/Aero application. Using a rugged VITA-based, Eurocard format, high-speed connectors, and design for interoperability, OpenVPX offers plenty of attractive features. With the multi-gigabit speeds, testing/simulation is required in many cases. Tools such as universal RTMs, VPX Cabling, and SerDes test devices will help engineers tackle the challenges in working with these high-performance systems.

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