IP to the Pin

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For decades, the electronics industry has pursued its version of the Holy Grail – concurrent design and test. Many have believed this an unattainable goal, considering how far apart the two worlds appear. In the design world, most engineers design at a system level using the latest electronic design automation (EDA) software, which has seen tremendous innovation over the last decade. The test industry has not innovated as quickly, and many companies have chosen to invest more in their design tools than their test engineering tools. The consequence is test engineers are typically outmatched when testing the latest software-centric electronic devices.

Pundits in every major industry have envisioned solutions to bridge this gap. In the semiconductor industry, experts have recommended the solution of protocol-aware test, visionaries in the U.S. Department of Defense (DOD) have proposed synthetic/virtual instrumentation, and the automotive industry has adopted hardware-in-the-loop and model-in-the-loop test. A closer look at all of these reconfigurable instrumentation architectures reveals some common themes: a system-level approach, the integration of design and test concepts, and the extension of software architectures into field-programmable gate arrays (FPGAs).

The next phase in integrating design and test is the ability for engineers to deploy design building blocks, known as intellectual property (IP) cores, to both the device under test (DUT) and the reconfigurable instrument. This capability is called “IP to the pin” because it drives user-defined software IP as close to the I/O pins of next-generation reconfigurable instruments as possible. The software IP includes functions/algorithms such as control logic, data acquisition, generation, digital protocols, encryption, math, RF, and signal processing.

To reuse IP requires both design and test engineers to operate at a certain level of abstraction and use a common design methodology. This technique is represented by the “V diagram,” where each phase of design has a corresponding verification or test phase. In this way, design and test teams can work their way “down the V,” from the highest-level modeling and design to lower-level implementation, and conduct tests at each stage.

For example, a multiple-input, multiple-output (MIMO) system on a chip (SOC)

includes receivers, transmitters, converters, filters, switches, and a processor (see figure 1). In addition, this SOC features software IP such as coding, modulation, encryption, and communication protocols. To fully validate the functionality of the highly integrated hardware and software subcomponents of the SOC, engineers need system-level test capabilities to effectively emulate another communication device in the system, such as a base station. Because many of the IP blocks of the DUT and the test system are common, this presents an ideal case for concurrent design and test with IP reuse.

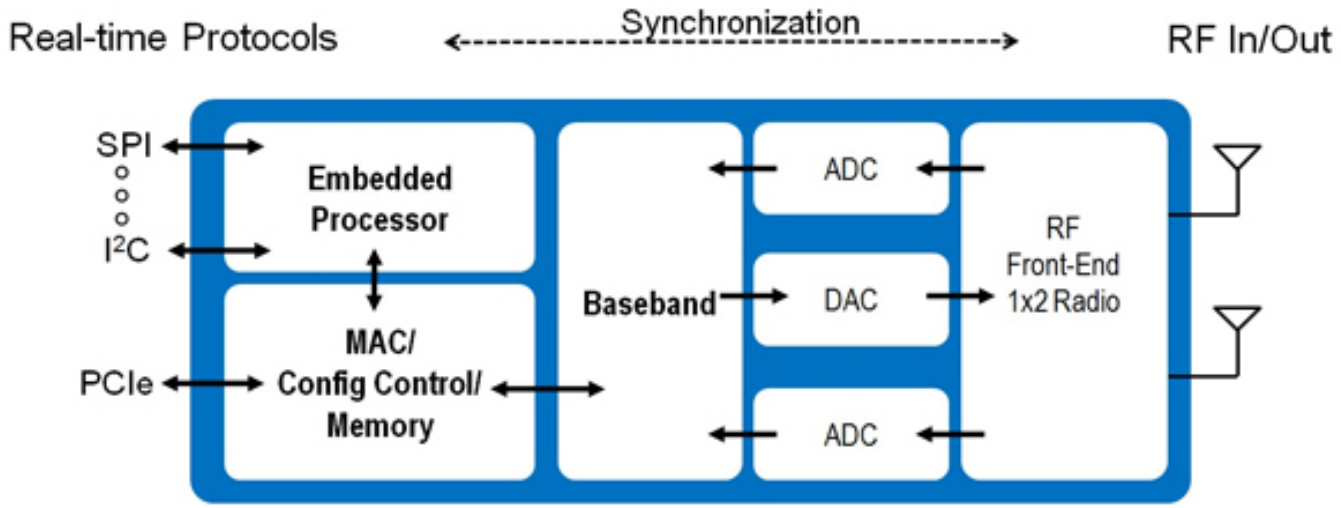

Figure 1. Example block diagram of an 802.11n WLAN System on a Chip (SOC)

The ability of a test engineer to directly embed the SOC design IP in the test instrumentation to perform system-level test can dramatically shorten design verification/validation and improve production test time and fault coverage. There are two key trends that will enable future reconfigurable test systems to deliver this IP-to-the-pin capability: the market shift toward FPGAs and the availability of high-level software to program them.

The electronics market is shifting to using an FPGA-based architecture for both electronic devices and test instrumentation. Moore’s law has become a proxy for the tremendous increases in performance and reductions in cost for all semiconductor devices and electronics products. Besides the microprocessor, FPGAs have probably benefited the most from Moore’s law because they have drastically increased in logic cell counts and functionality and decreased in cost per transistor. Engineers can now pack additional software IP in a single FPGA.

Vendors are also beginning to integrate FPGAs with devices such as processors, data converters, and transceivers to deliver increased performance and user programmability even closer to the I/O pin. This trend is made possible by Moore’s law rendering the cost and size of programmable gates to nil. All of these advancements have brought FPGA capabilities more in line with those of an ASIC. This performance boost and the empirical advantage of being reprogrammable in software have created a market shift toward FPGA-based designs over the last decade for electronic devices. In a 2009 report, the Gartner research firm stated

that FPGAs now have a 30 to 1 edge in design starts over ASICs. Every industry and application area is adopting FPGAs including consumer electronics, automotive electronics, and military/aerospace technology. Moshe Gavrielov, CEO of Xilinx, has called this migration to FPGAs “the programmable imperative.”

Because of the programmable imperative, design engineers can turn to higher levels of abstraction in designing semiconductors and electronic systems. Increasingly, they are able to reuse existing FPGA IP as building blocks of a new design. Because of this abstraction, they can design at a system level and get new products to market with new features faster than ever before. This leads to the second market trend: the increase in availability and capability of high-level synthesis (HLS) tools for test engineers. These HLS tools provide an automated process that interprets an algorithmic description of a desired behavior and creates FPGA logic that implements that behavior. This abstraction increases the accessibility of FPGA design to more engineers and provides a platform for programming at a system level.

There are also emerging multivendor IP ecosystems that feature IP cores from all major FPGA vendors as well as their software and instrumentation partners. The National Instruments FPGA IPNet and the Cadence/Xilinx IP microsites are examples of these ecosystems. They contain hundreds of IP blocks and functions, including the Xilinx CORE Generator, serial communication protocol cores, and Advanced Encryption Standard (AES) components as well as peer-to-peer streaming algorithms.

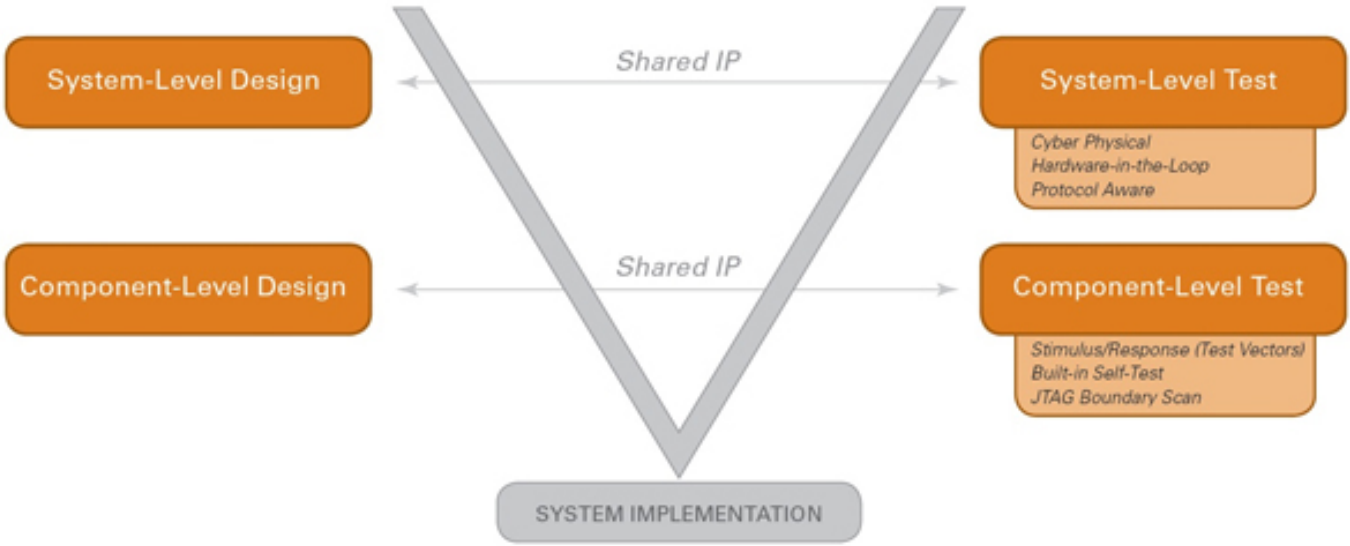

Figure 2. Sharing common FPGA IP between design and test dramatically shortens design validation and improves production test time and fault coverage.

These trends deliver design and test engineers the capabilities required to reuse IP and enable concurrent design and test (see figure 2). Moving forward, companies need to adopt an investment strategy that provides design and test engineers with comparable capabilities. In doing so, they can achieve the maximum business impact including shorter time to market, higher quality, and more profit.

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