3D Integration of Power MOSFETs Drives Performance in Low-voltage Synchronous Buck Converters

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Efficiency and power loss in microelectronic devices is a major issue in power electronics applications. The engineers are challenged every year to increase power density and at the same time reduce the amount of power dissipated in the applications to keep the maximum temperatures under specifications. This situation drives a constant demand for better efficiencies in smaller packages. Traditional approaches to improve efficiency in DC/DC synchronous buck converters include reducing conduction losses in the MOSFETs through lower RDS(ON) devices and lowering switching losses through low-frequency operation. However the incremental improvements in RDS(ON) are at a point of diminishing returns, and low RDS(ON) devices have large parasitic capacitances that do not facilitate the high-frequency operation required to improve power density.

The drive for higher efficiency and increased power in smaller packages is being addressed by advancements in both silicon and packaging technologies. A new Power Block MOSFET offering combines these two technologies to achieve higher levels of performance, and in half the space versus discrete MOSFETs. This article explains these new technologies and highlights their performance advantage.

Reduce Switching Losses

The major losses that occur within a MOSFET switch in a typical synchronous buck converter consist of switching, conduction, body diode and gate drive losses. The switching losses are primarily caused by the parasitic capacitances formed within the structure of the device. The conduction losses are a result of the device’s resistance (RDS(ON)). The body diode losses are a function of its forward voltage and reverse recovery (Qrr). Gate drive losses are determined by the Qg of the MOSFET. Therefore, the parasitic capacitances and the RDS(ON) determine the efficiency of the device. The most common technology used in today’s low-voltage MOSFETs is the Trench-type MOSFET (Figure 1). They can achieve very low resistance but, unfortunately, the large area of the trench walls makes it difficult to keep the internal capacitances small. The resulting high capacitances force designers to choose between a low operating frequency to optimize the efficiency and high frequency with better power density.

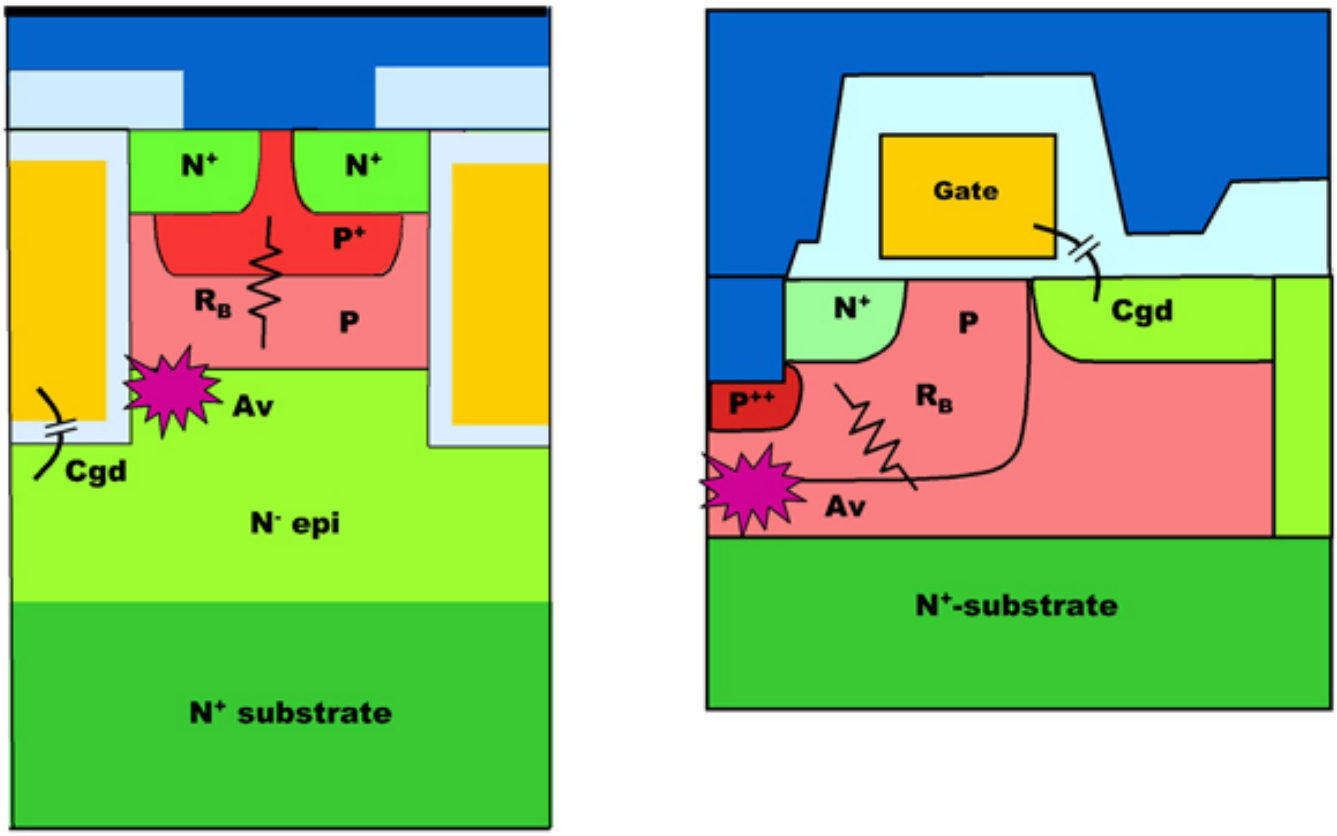

Figure 1. MOSFET structure comparison. Trench MOSFET (left) and NexFET (right).

In 2007, the NexFET power MOSFET was introduced. The NexFET can achieve similar specific on resistance to the Trench technology while reducing the associated parasitic capacitances by about fifty percent. The NexFET device finds its roots in a laterally diffused MOSFET (LDMOS) and combines vertical current flow to achieve high-current density. A closer look at the structure (Figure 1) reveals that the area underneath the gate has minimum overlap over source and drain regions keeping the internal capacitances small. The reduced capacitances result in lower charges (Qg, Qgs, Qgd) required to switch the device. Therefore, the device switches faster, reducing the switching losses within the MOSFET. Because less energy is required from the drive circuit, the losses in the driver are also reduced.

Reduce Space and Parasitic Impedances

In order to maximize the performance of a typical synchronous buck converter, we need to minimize the parasitic inductances and resistances in the package. This is accomplished through an innovative approach in the power block where the MOSFETs are actually stacked on a grounded lead frame with two copper clips (Figure 2). The resulting power block package has characteristics that make it unique in the power electronics industry. The package accomplishes four primary functions: small footprint, very low parasitics, excellent thermal performance, and solid reliability.

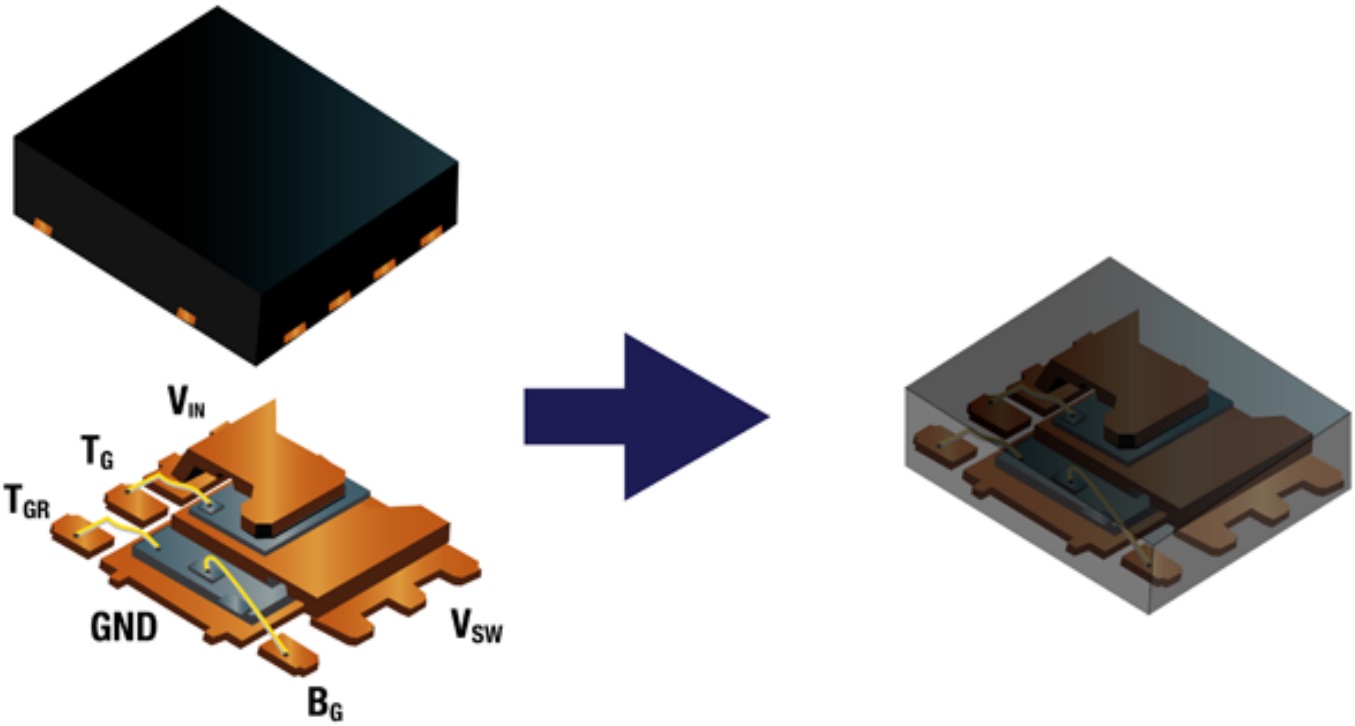

Figure 2. The source down technology allows the MOSFETs to be stacked.

To achieve a small footprint and the lowest parasitics possible, a stacking topology was used in the power block package design. A source down silicon technology was developed to allow the stacking of the high-side die on top of the low-side transistor to implement a synchronous buck converter topology in a very simple and cost-effective manner. The low-side die is attached to the main pad of the lead frame providing the ground connection of the MOSFET pair (Figure 3). The drain of the low-side is connected to the outside through a thick copper clip that constitutes the switching node of the device (VSW). On top of the thick copper clip, we solder die attach the high-side MOSFET (which also uses a source down technology). Finally, another thick copper clip connects the drain of the high side (VIN of the Buck converter) to the external pins of the device. The gate connections are made using two Au wire bonds (TG and BG) and TGR is the top gate return to the IC driver. TGR is a sense signal of the switching voltage node that allows the IC driver to properly bias the gate of the high-side MOSFET.

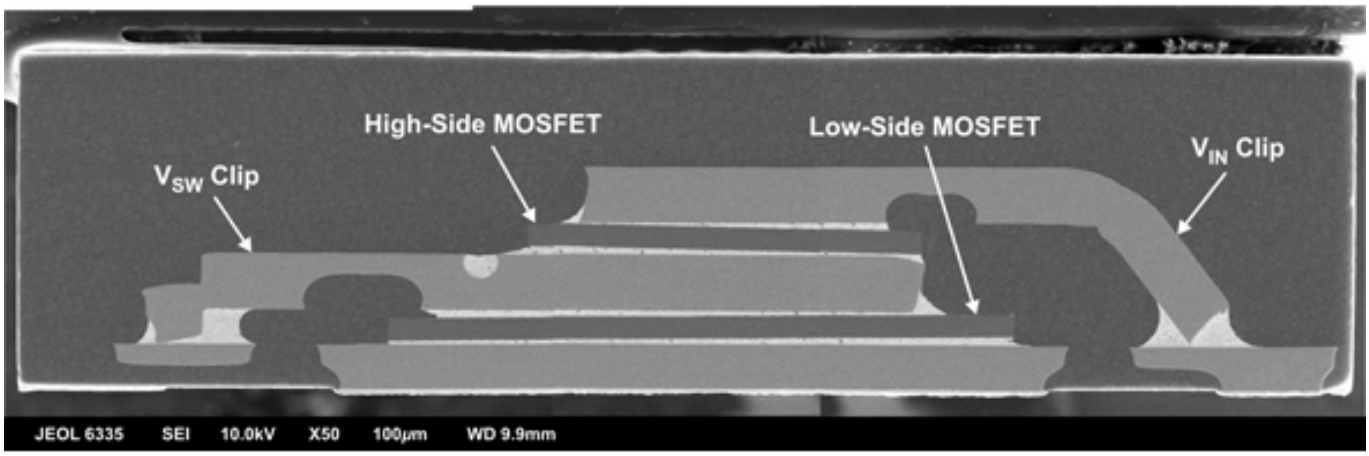

Figure 3. A cross sectional view of the power block illustrates the unique packaging approach.

Maximizing Performance and Density

Combining the source down NexFET technology and the stacked die packaging technique significantly reduces the associated parasitics and creates a synchronous buck power block capable of outperforming discrete MOSFET transistors. The 5 mm x 6 mm power block (CSD86350Q5D) achieves over two percent higher efficiency at 25 A than two discrete NexFETs with similar conduction and switching characteristics (Figure 4). Efficiency peaks at over 93 percent and is 90.7 percent at 25 A. The higher efficiency translates into more than a 20 percent reduction in power loss. The reduced power loss improves thermal performance and reduces system operating costs, or it can be used to enable higher frequency operation to improve power density.

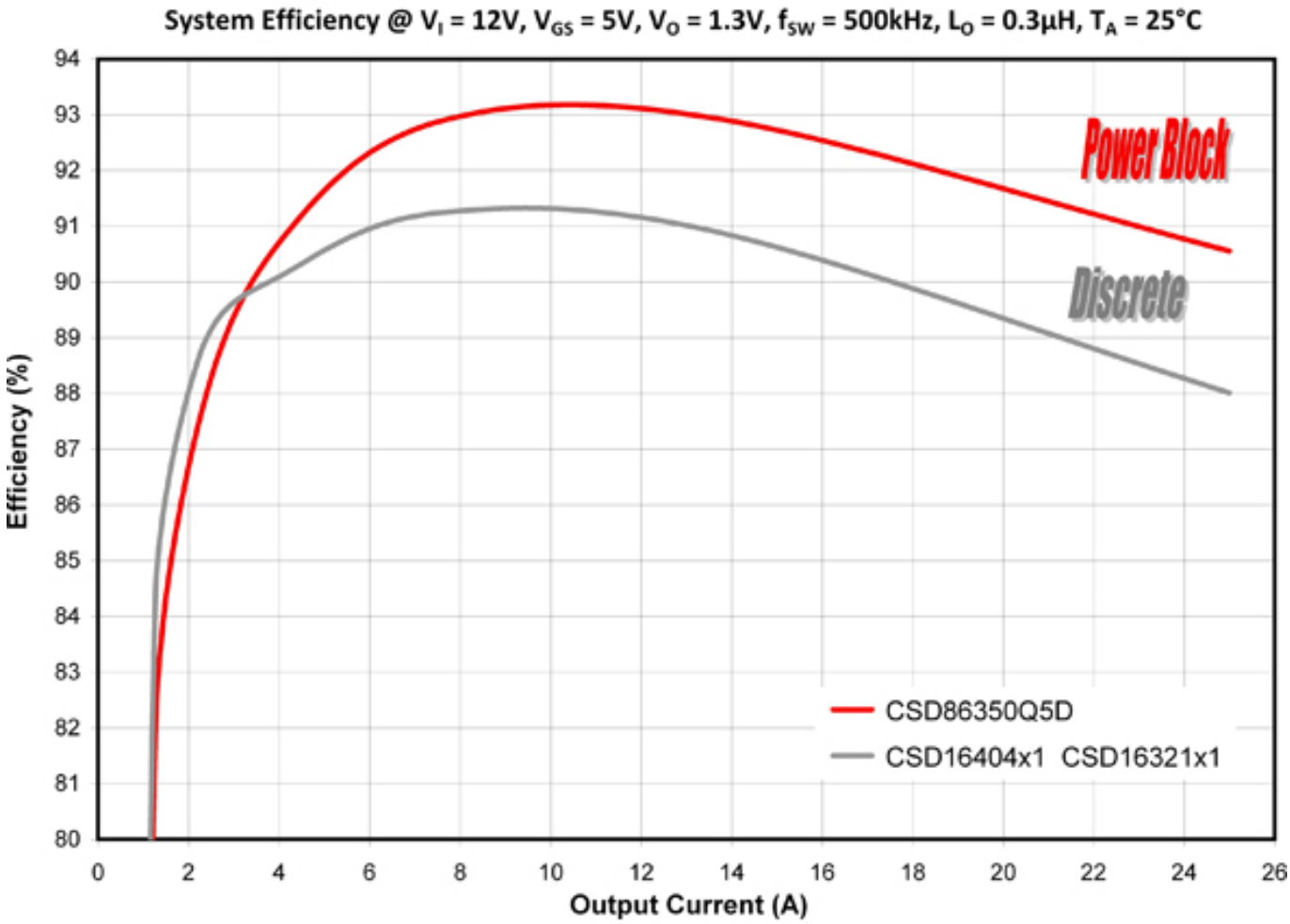

Figure 4. The NexFET 5 mm x 6 mm power block significantly improves efficiency over similar discrete MOSFETs.

The 3 mm2 power block (CSD86330Q3D) combined with the TPS53219 pulse-width modulation (PWM) controller, for example, achieves high performance while using only 20 mm2 of printed circuit board (PCB) area. The controller uses D-CAP mode, which eliminates the need for an external compensation network while achieving excellent transient response. This reduces the number of external components and further improves the point-of-load (POL) power density. A closer look at the efficiency curves in Figure 5 shows that the combination of the TPS53219 and the 3 mm2 power block converts 12 V to 2.5 V at 93 percent efficiency with an output current of 15 A. Peak efficiency reaches 95 percent. Even with an output voltage of 1.5 V, the measured system efficiency is 89.8 percent at 15 A with a peak of 92.5 percent.

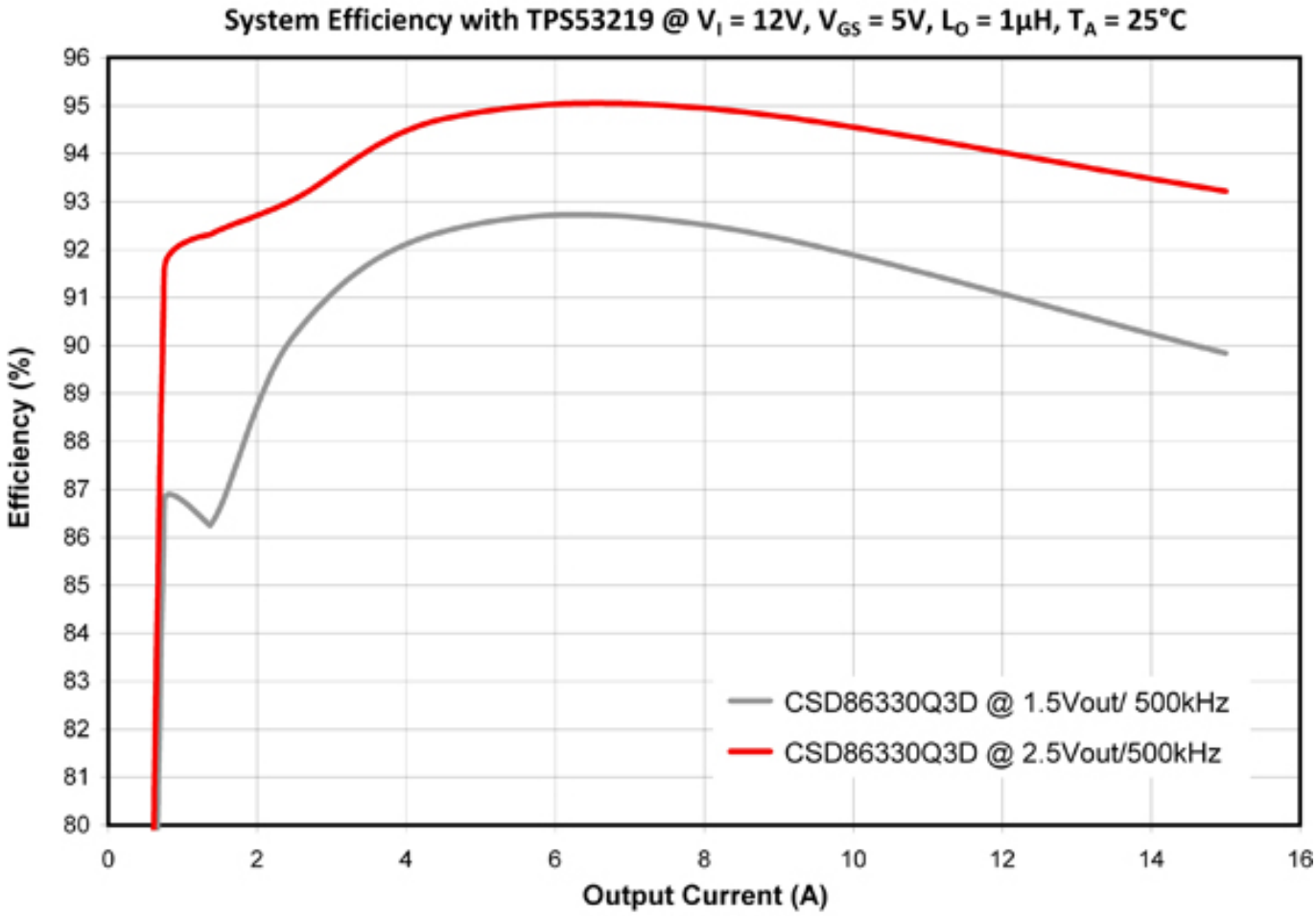

Figure 5. The NexFET 3 mm2 Power Block combined with a 3 mm2 WM controller achieves high efficiency and power density.

Beyond improving performance and reducing board space by 50 percent versus discrete MOSFETs, the NexFET Power Block simplifies the development effort. In discrete implementations, care must be taken in the layout when connecting the two devices to reduce inductance; now this concern has been eliminated. The pin-out allows easy placement of discrete components. This includes locating input capacitors close to the package, and the output inductor with the noise generating switch node on the opposite side of the package from the input capacitor and PWM controller IC. The NexFET Power Block also benefits from a grounded lead frame that should improve thermal performance and reduce electromagnetic interference (EMI). All of these attributes can help designers achieve first-time success when designing with the NexFET Power Block.

References

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For more information about NexFETTM technology, visit: www.ti.com/nexfet-ca [1].

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