Low MOSFET Gate Resistance – A Key requirement for Improving Efficiency of DC-DC Converters

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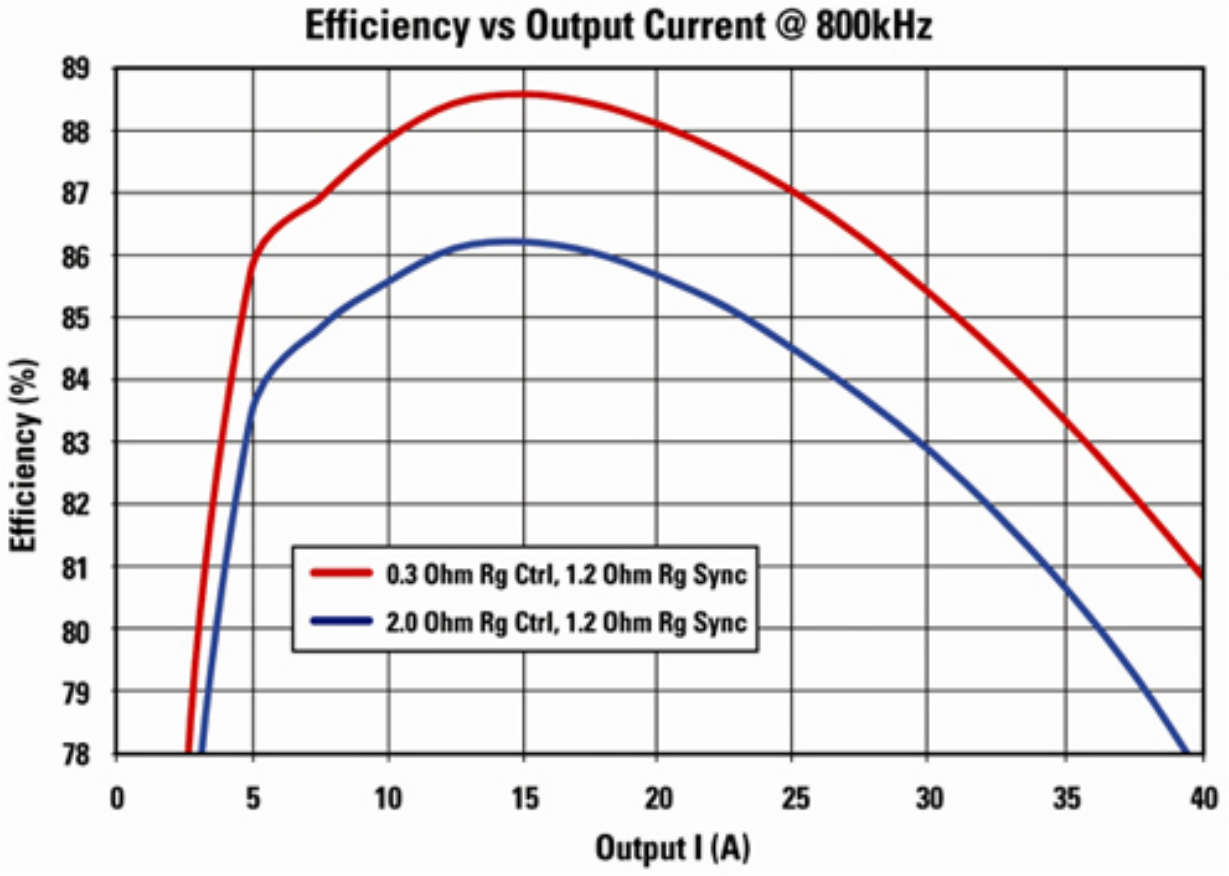
Improvements in Si MOSFET technology, particularly in the last decade, have enabled significant reduction in power consumption of servers, notebook, desktops and other computing devices. These improvements were realized by minimizing key MOSFET parameters like, On-resistance Rds(on) and Gate Charge (Qg), and resulted in synchronous-buck converter efficiencies over 90 percent. With the reduction of these parameters with successive generations of Si MOSFET technology, continued improvement in DC-DC converter efficiency also depends on other MOSFET parameters largely ignored previously. One such key parameter is gate resistance (Rg) of the MOSFET.

As a practical illustration, Figure 1 shows the dramatic impact of Rg of the control FET as operating frequency is increased from 300 kHz to 800 kHz.



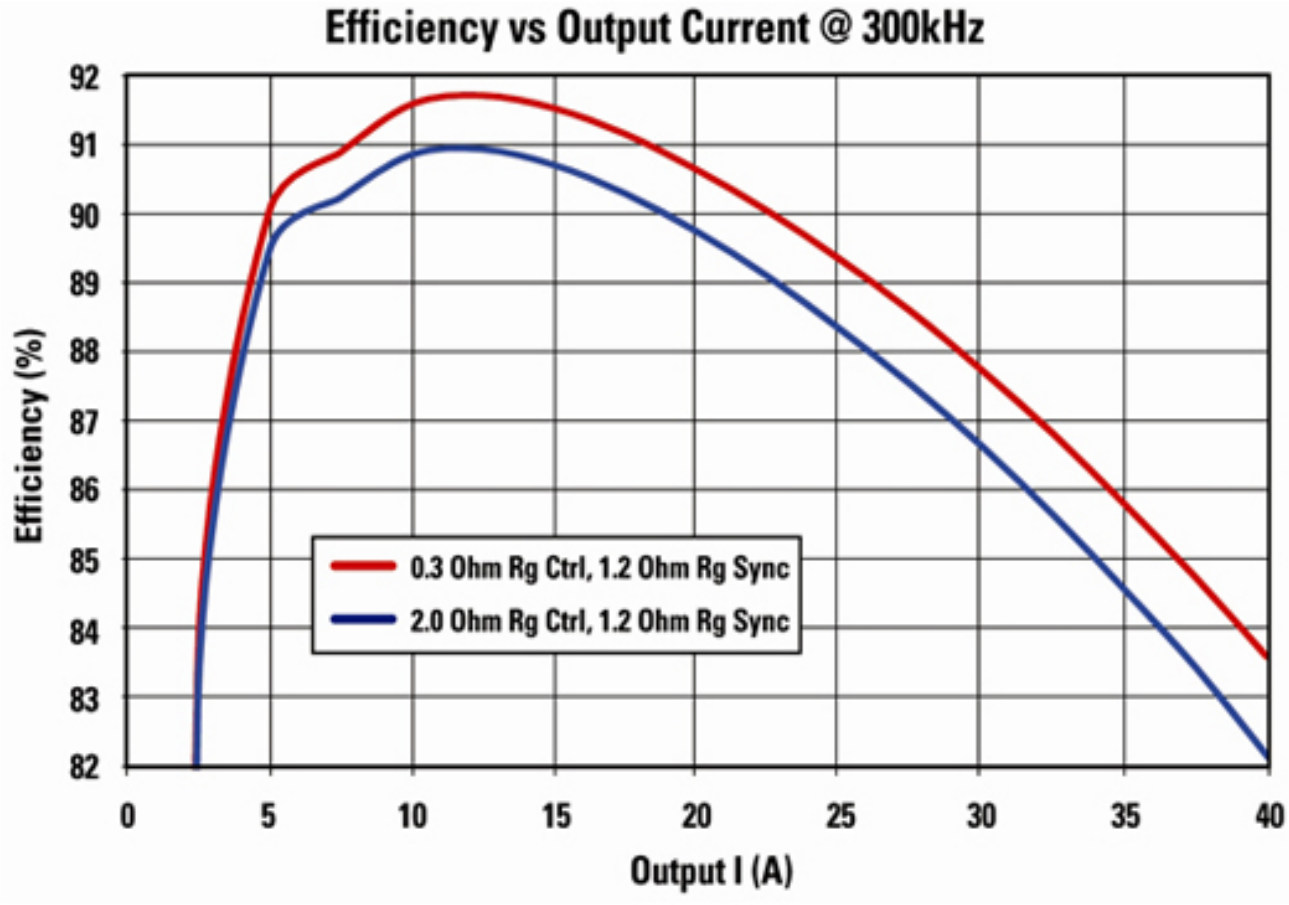


Figure 1. Efficiency measurements at 300 kHz and 800 kHz.

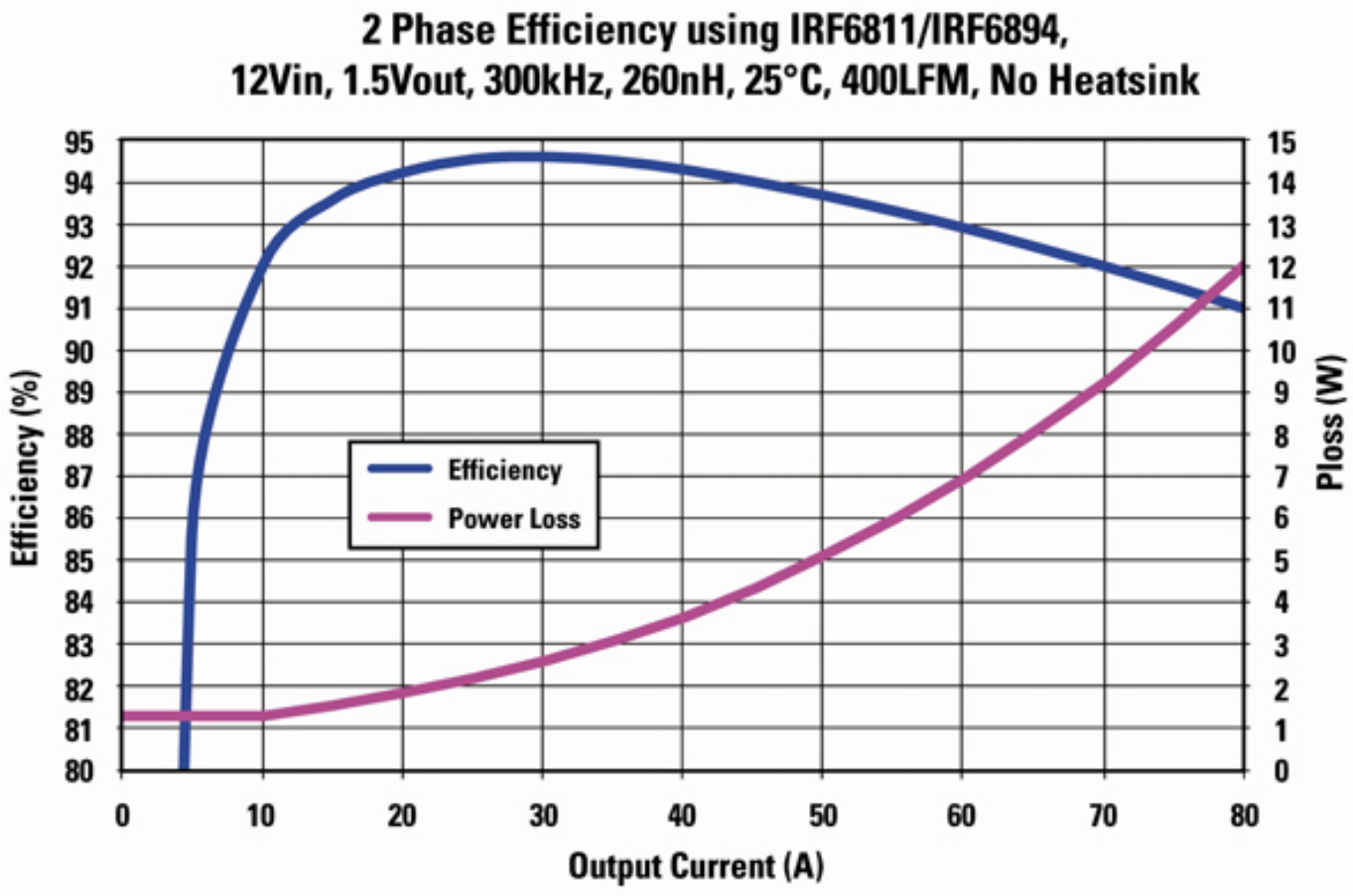
The improvement in efficiency with lower Rg can be attributed to reduced switching loss associated with the control FET. A similar impact can be achieved by reducing Qg, however, lowering Qg typically results in a trade off with Rds(on) and therefore is less effective compared to lowering Rg.

Lowering Rg is also effective in preventing Cdv/dt induced turn-on of the sync FET, which occurs due to the rapid increase in sync FET drain voltage due to the control FET turning on. The rapidly increasing voltage induces a voltage spike on the sync FET gate through its miller capacitance, which could potentially turn the sync FET on. This Cdv/dt induced turn-on causes significant power loss impacting efficiency throughout the load range. A low gate resistance Rg effectively minimizes this gate spike thereby eliminating this loss mechanism.

A lower Rg enables better matching of the gate driver output impedance. With the continued emphasis on improving efficiency, it is becoming increasingly clear that further improvement will require more of a system approach than just improving MOSFET Rds(on) and Qg. In particular, the synergy between the gate driver characteristics and the MOSFETs it drives, is key to optimizing efficiency. Ability to modulate Rg to effectively match the driver output impedance improves its drive capability and hence efficiency.

A further benefit of lowering Rg is improved reliability. MOSFET typically comprise of large numbers of cells connected in parallel. Ensuring more uniform turn-on characteristics for the individual cells avoids temporarily exposing a reduced number of cells to the full load current, thereby improving reliability.

IR’s latest generation of DirectFET Plus MOSFETs feature IR’s latest generation of Si technology with significantly lower Rds(on) and gate charge (Qg) compared to previous generation devices to significantly reduce power loss up to 25 percent. In addition, the devices offer all the benefits associated with ultra low gate resistance (Rg) thereby enabling further efficiency improvement by minimizing switching losses in DC-DC converters.



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