What Gives at Dropout? Low dropout regulator performance near dropout

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This article explains how the performance of the PMOS low-dropout (LDO) regulator changes when the input-to-output voltage is decreased to approach the dropout voltage. Specifically, the effect on key electrical characteristics will be discussed: line and load regulation, power supply rejection ratio (PSRR), control loop stability and transient response, and quiescent current. These performance changes can be generalized across all other linear regulators based on NMOS, and bipolar pass transistor architectures.

Introduction

Figure 1 shows the simplified block diagram for an LDO regulator and its external circuitry. The LDO circuit functions as a control loop to provide a DC-regulated voltage, V_{OUT}, at the load, R_{load}, by controlling current through the pass FET. The loop gain is the product of the voltage divider gain (?=R2/(R1+R2)), the gain of the error amplifier (Ga), and the voltage gain of the common source, FET amplifier ($G_F = g_m*(r_o ||(R1+R2)||Zo)$), where g_m is the transconductance gain of the FET.

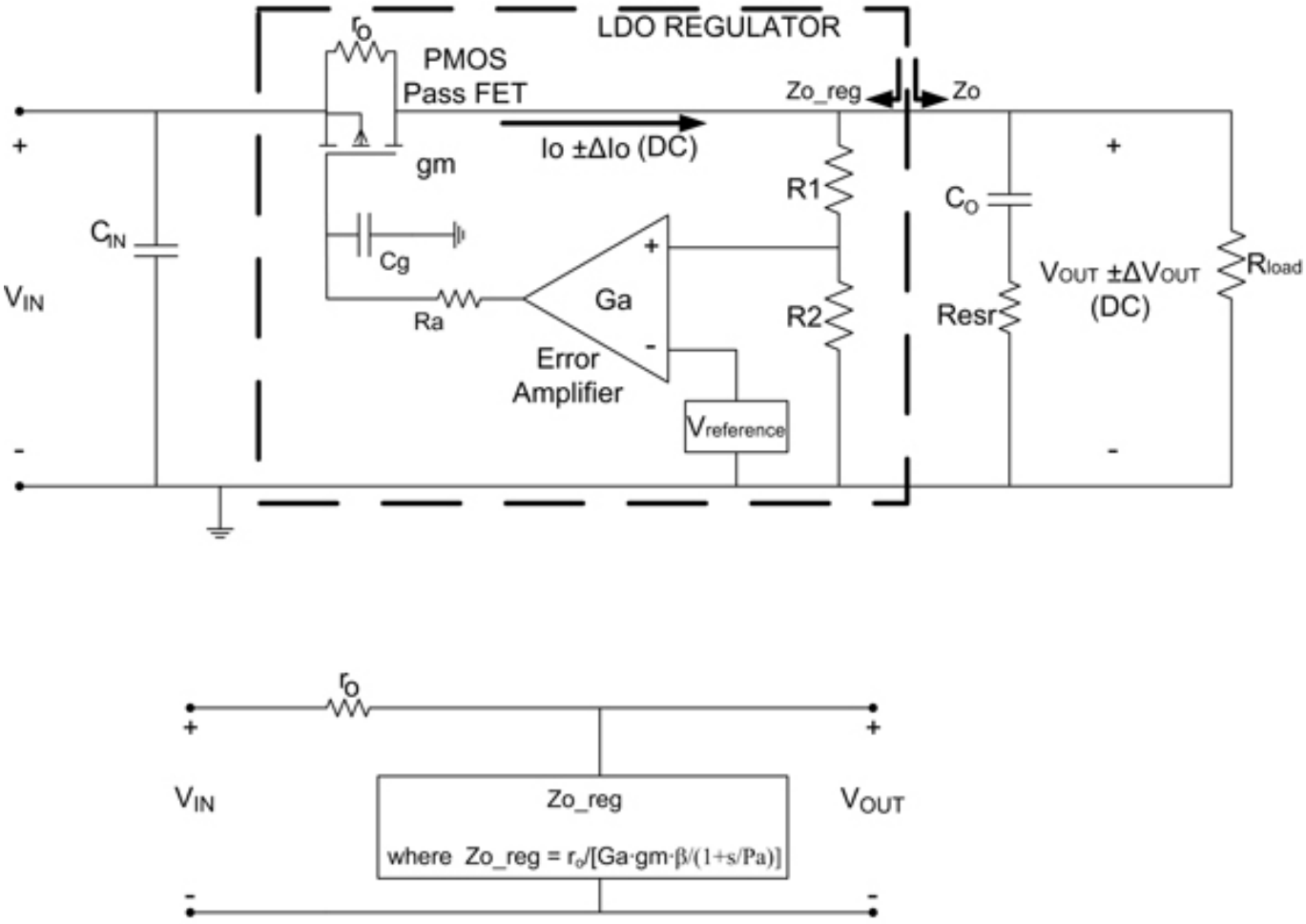


Figure 1. Basic LDO circuit diagram.

The ability of the control loop to achieve characteristic specifications is a function of the designed loop bandwidth, loop gain, accuracy of the reference voltage, and significantly, the region of operation of the pass FET: the saturation region or the linear region approaching dropout (V_{DO}). Operating the LDO with the FET biased in active saturation region affords optimal AC performance of the loop while operation in the linear (ohmic) region, near dropout, yields poorer performance, albeit better efficiency.

Figure 2 depicts a set of characteristic curves for a MOSFET, essentially similar to those for the pass FET of the LDO. As the drain-source voltage is decreased, from operating point P1 the pass FET transitions from its saturation region, through its linear region beginning at P2, to finally reach the dropout voltage (V_{DO}) at P3 where the FET acts only as a linear, drain-source resistance. In the saturation region the voltage gain of a FET amplifier is maximum due both to the high transconductance gain (g_m = ?I_{ds}/?V_{gs}) shown as an increasing function of drain-source current, and the high output impedance, ro, illustrated by the flat, similarly sloped curves. In the linear region the physics of the transistor change: the FET changes from a transconductance gain stage to something like a voltage controlled resistor stage. This effect is illustrated by the narrower spacing between curves that are indicative of very low transconductance. The wider variations in slope are indicative of multiple resistances. For an LDO with its pass FET at dropout, its input-output

resistance, ro, is at minimum, the gate-source drive voltage is at maximum limit, and the LDO ceases to regulate the output ($V_{OUT} = V_{IN} - I_O$*Rdson, where Rdson is r_o at minimum).

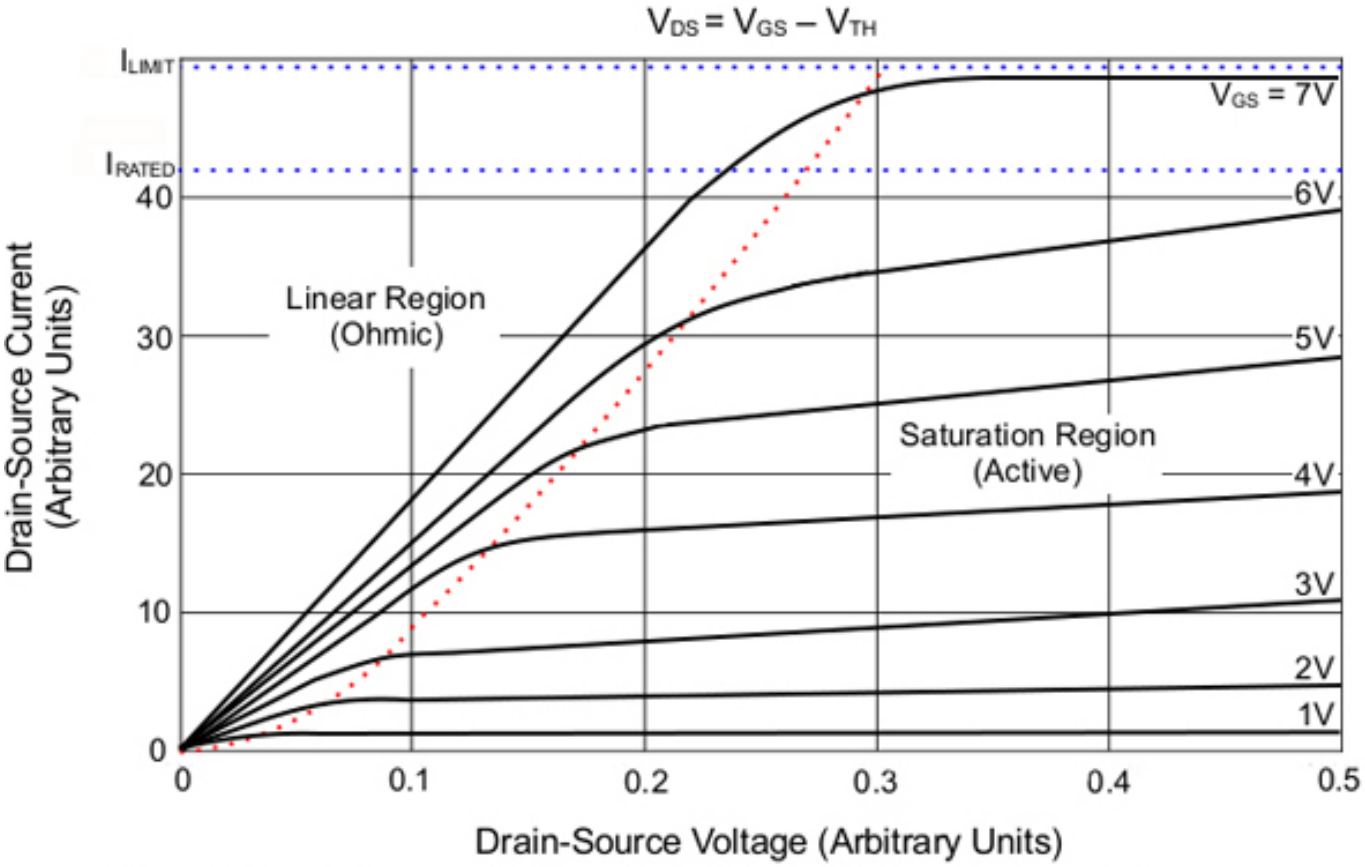


Figure 2. Typical pass FET characteristic curves showing the relative dependence of the drain-source current, Ids; on gate-source voltage, Vgs; and drain-sourse voltage, Vds.

DC load and line regulation near dropout

The DC or low-frequency model for an LDO can be understood from Figure 1, but with all reactive, or capacitive, components removed. This greatly simplifies the analysis.

DC load regulation

Load regulation expresses the degree to which the regulated output voltage changes after a change to the load current. When the DC load changes from I_{OUT} to I_{OUT} ±?I_{OUT}, then the nominal output voltage changes by some ?V_{OUT} dependant on the DC loop gain alone per Equation 11:

$$\Delta V_{OUT} / \Delta I_{OUT} = (1 / gmG_a\beta) \qquad \text{(Equation 1)}$$

The larger the product of the tranconductance gain, the error amplifier gain and the voltage divider gain, the smaller will be the output error, ?V_{OUT}, for a given change

in I_{OUT}. As the input-output voltage decreases toward dropout, the gm decreases as the pass FET nears the linear region. This tends to increase the output error, $?V_{OUT}$. For the well designed LDO, the error amplifier gain, G_a, is sufficiently large to guarantee regulation (usually by a wide margin) until the drain-source voltage is very near to the dropout voltage. At dropout, the gate drive reaches its operational limit and the LDO stops regulating, the output voltage decreases with the input voltage minus the resistive voltage drop across the pass FET.

DC line regulation

Line regulation expresses the degree to which the regulated output voltage is influenced by a change to the input voltage, V_{IN}. When the DC input line voltage changes to $V_{IN} \pm ?V_{IN}$, then V_{OUT} will again change by some $?V_{OUT}$ in accord with Equation 2[1].

$$\Delta V_{OUT} / \Delta V_{IN} = (1/((r_O + R_{load}) gm G_a \beta) \qquad \text{(Equation 2)}$$

As the LDO approaches dropout, both the transconductance gain, g_m, and the output impedance of the pass FET, r_O, decrease causing the $?V_{OUT}$ error to increase. For the typical LDO the overall loop gain allows the output to stay within specified regulation limits up to the point of dropout.

Power supply rejection ratio

The PSRR is the ability of the LDO control loop to reject input ripple (e.g., 1Hz to 10MHz) on the V_{IN} rail by maintaining the output ripple-free, V_{OUT}. The PSRR function of the loop can be approximated at lower frequencies by modeling the LDO in isolation from its output impedance as a voltage divider circuit[3]. This is seen in **Figure 4** as the impedance from input to output, r_O, and then the impedance of the regulated output to ground, Zo reg The PSRR has been derived in **Equation 3** for the model shown in **Figure 4**[2]. The loop gain is bandwidth limited by the intenal pole, P_a, caused by R_a and C_g (see **Figure 1**) of the LDO (where $P_a = 1/2?R_aC_a$).

$$PSR = (Z_{o\_reg}) / (r_o + Z_{o\_reg}) \approx (1 + s / P_a) / (G_a gm \beta (1 + s / (P_a * G_a gm \beta) \qquad \text{(Equation 3)}$$

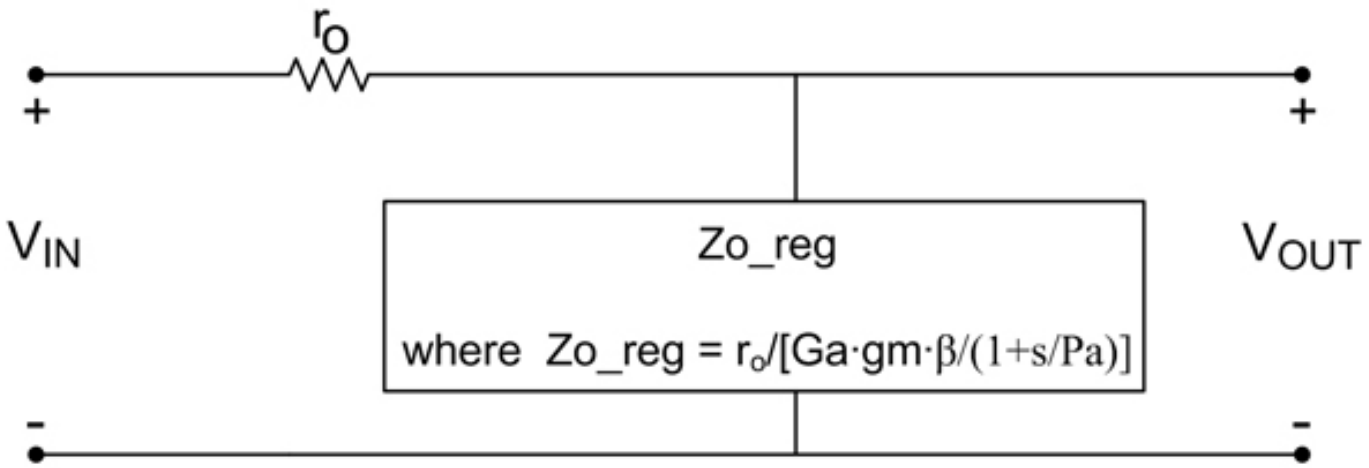


Figure 3. Low-frequency PSRR model where the output impedance can be ignored.

According to this model the PSRR is entirely a function of the loop gain and the one internal pole, P_a.

As the input-output voltage is reduced to near dropout the PSRR decreases dramatically (logorithmically) due to the reduction in transconductance gain of the pass FET, the reduced effect of the gate-source voltage on the drain current, and finally the inability of the error amplifier to vary the drain current near dropout. **Figure 5** shows a set of typical PSRR plots, in this case for a TPS79501 LDO, illustrating the reduction in gain as the input-output voltage approaches full-load dropout (where V_{DO}= 110mV). These plots show our model of **Figure 3** to be good to about 100kHz.

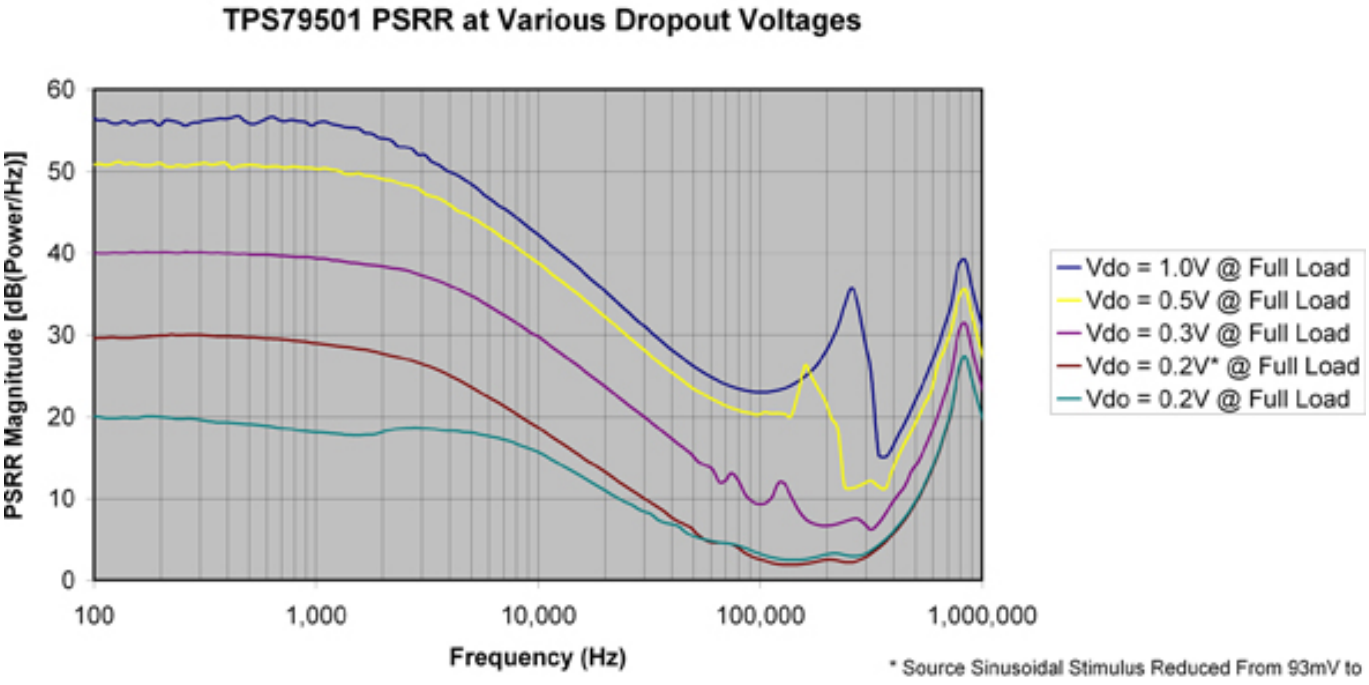


Figure 4. PSRR plots showing the effect of decreasing dropout voltage on loop gain.

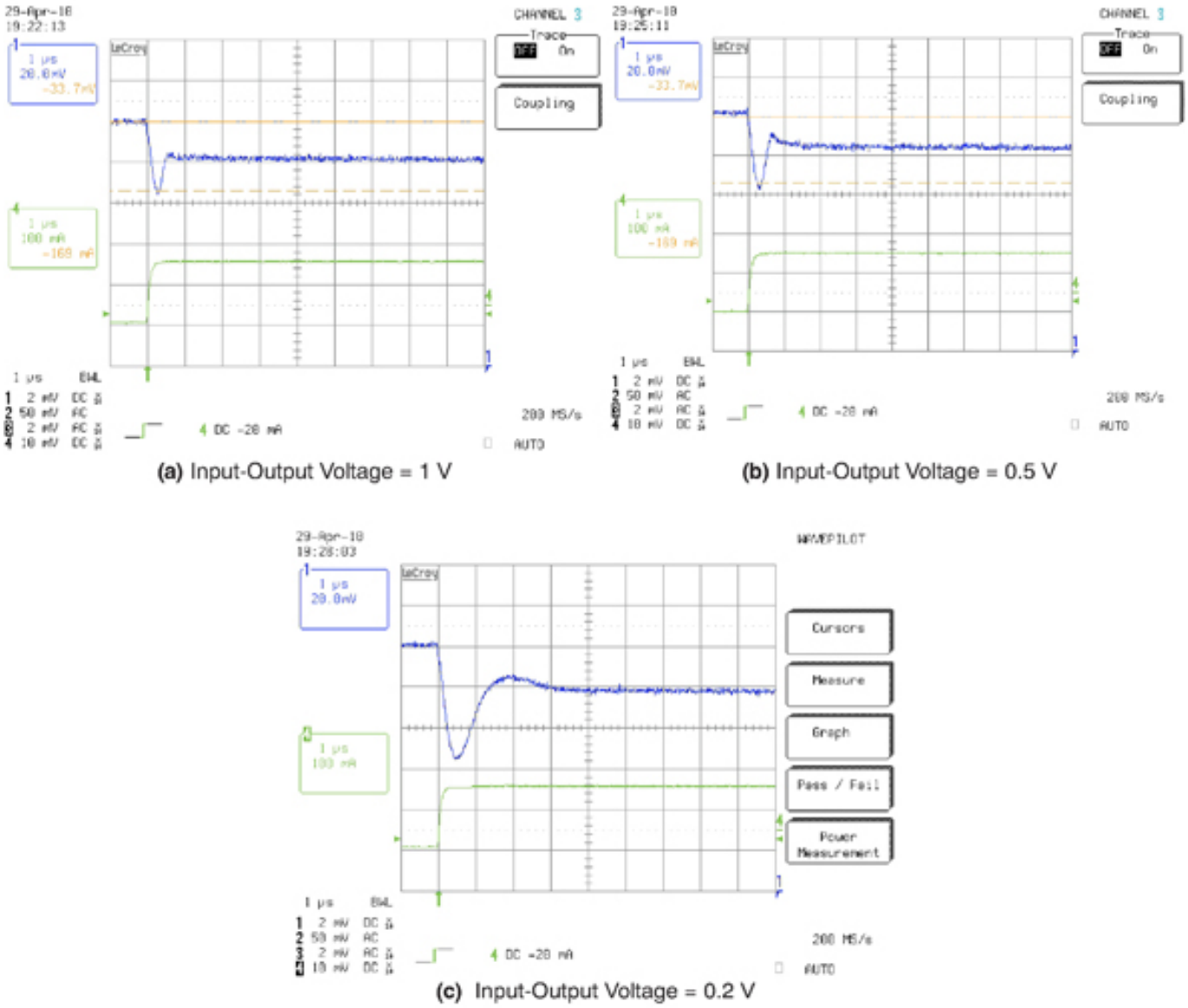
Loop stability and load transient response

The control loop for most recent LDOs consists of multiple, embedded loops with provision for small and large signal behavior. But the basic loop model will suffice here. **Equation 4**[3] gives the simplified open loop gain equation, G_{OL}, based on the PMOS LDO of **Figure 1**.

$$G_{OL}(s) = \beta \cdot G_a \cdot gm \cdot R_p \cdot (1 + sC_O R_{esr}) / ((1 + sC_g R_a) \cdot (1 + sC_O (R_p + R_{esr})) \quad \text{(Equation 4)}$$

where $R_p = r_O \,||\, (R1+R2) \,||\, R_{load}$ and ?=R2/(R1+R2).

Decreasing the input-output voltage to approach dropout reduces the loop gain, bandwidth, and shifts the output pole frequency ($F_{P\_OUT} = 1/2?C_O(R_p+R_{esr})$). Though it is beyond the scope of this article, **Equation 4** shows that typically a reduction in gain will improve stability (i.e., phase margin increases) while significantly slowing or worsening the step load transient response as bandwidth narrows. **Figure 5** illustrates this change in step response by employing the TPS71728 LDO to drive a step load from 45mA to 150mA for three cases where the input-output voltage is decreased toward the dropout voltage.



(a) Input-Output Voltage = 1 V

(b) Input-Output Voltage = 0.5 V

(c) Input-Output Voltage = 0.2 V

Figure 5. Step-load transient and output response. Oscilloscope channel 4 shows the load current step, and channel 1 shows the Vout transient response: a) for input-output voltage equal to 1.V; b) for input-output voltage equal to 0.5V; and c) for input-output voltage equal to 0.2V.

Quiescent current

As the input-output voltage is decreased to near dropout, the drive voltage to the gate of the pass FET and various other circuits is driven to their operating limits. At dropout, when all these internal circuits are saturated, there is often a large rise in quiescent current. Some higher end regulators, however, use balanced, differential drive circuitry that always draws the same current whether operating at drive limits or not.

Conclusion

The PMOS LDO performance is optimal when the input to output voltage difference is great enough to assure that the FET is operating in its saturation region. The transition between the saturation region and the linear region of FET operation is

not abrupt. As the input to output voltage is reduced to approach dropout, V_{do}, the transconductance gain of the FET rolls off, the output impedance of the FET decreases, and the gate-source drive reaches practical limitations to altogether reduce LDO performance.

References

1. Bang S. Lee, Technical Review of Low Dropout Voltage Regulator Operation and Performance [1], Application Report (SLVA072), Texas Instruments, August 1999.
2. Vishal Gupta, Gabriel A. Rincón-Mora, Prasun Raha, Analysis and Design of Monolithic, High PSR, Linear Regulators for SoC Applications [2], Georgia Institute of Technology, Texas Instruments.
3. Everett Rogers, Stability Analysis of Low-Dropout Linear Regulators with a PMOS Pass Element [3], Analog Applications Journal (SLYT194), Texas Instruments, August 1999.

About the Author

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