Low-Noise LDOs Offer Advantages for Noise Sensitive Analog and RF Applications

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Low dropout (LDO) linear regulators provide essential performance characteristics for many precision analog and mixed-signal applications including low noise, fast transient response, high power supply rejection ratio and small size. But the noise levels of conventional LDOs may not be low enough for noise-sensitive analog and mixed-signal circuits such as voltage controlled oscillators (VCOs), phase locked loops (PLLs), analog-to-digital converters (ADCs) and digital-to-analog converters (DACs).

Low noise is important for LDOs used in the analog environment because analog components are more sensitive to noise than digital devices. Analog LDO noise requirements are mainly driven by the wireless interface requirements: do no harm to the receiver or transmitter, and create no pop or hum in the audio system. Wireless connections are highly susceptible to noise, and a receiver’s sensitivity can be reduced if the noise interferes with the signal. Adding an external filter or a bypass capacitor can also reduce noise, but adds cost and increases the PCB solution size.

Fortunately, noise reduction and supply noise rejection can also be achieved by care and ingenuity in the internal design of the LDO. To set the stage, let’s briefly review LDO technology. The LDO is designed to maintain a specified output voltage under a wide range of load currents and input voltages including very small differences between input and output voltages. This difference, known as the dropout voltage, can be as low as 80 mV at 200 mA. An LDO consists of a voltage reference, error amplifier, feedback voltage divider and pass transistor. Output voltage is delivered via the pass transistor. Its gate voltage is controlled by the error amplifier, which compares the reference voltage with the feedback voltage, amplifying the difference to reduce the error voltage.

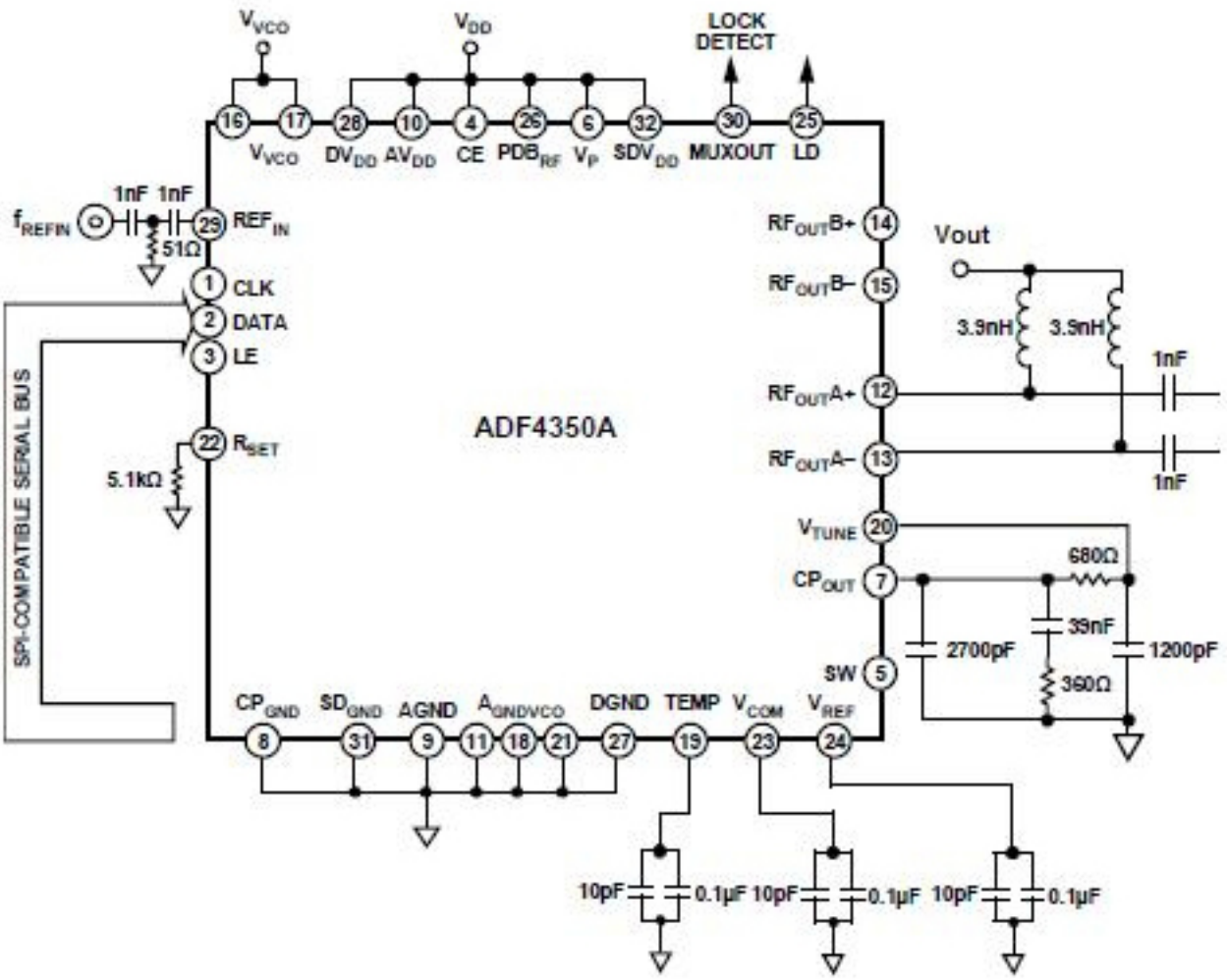

Figure 1. Typical VCO+PLL requires three power supplies.

As an example of a noise sensitive device, we will look at the ADF4350A VCO+PLL, which requires three power supplies as shown in Figure 1. Here is the maximum supply current for each voltage domain.

Vdd = AVdd + DVdd + SDVdd + Vp = +3.3 V
DIdd + AIdd + SDIdd + Ip = 27 mA max

Vout = +3.3 V
IRFOUT(A+/A-) = 26 mA max
IRFOUT(B+/B-) = 26 mA max
Total 52 mA max

Vvco = +3.3 V
Ivco + Ioutdiv = 86 mA max

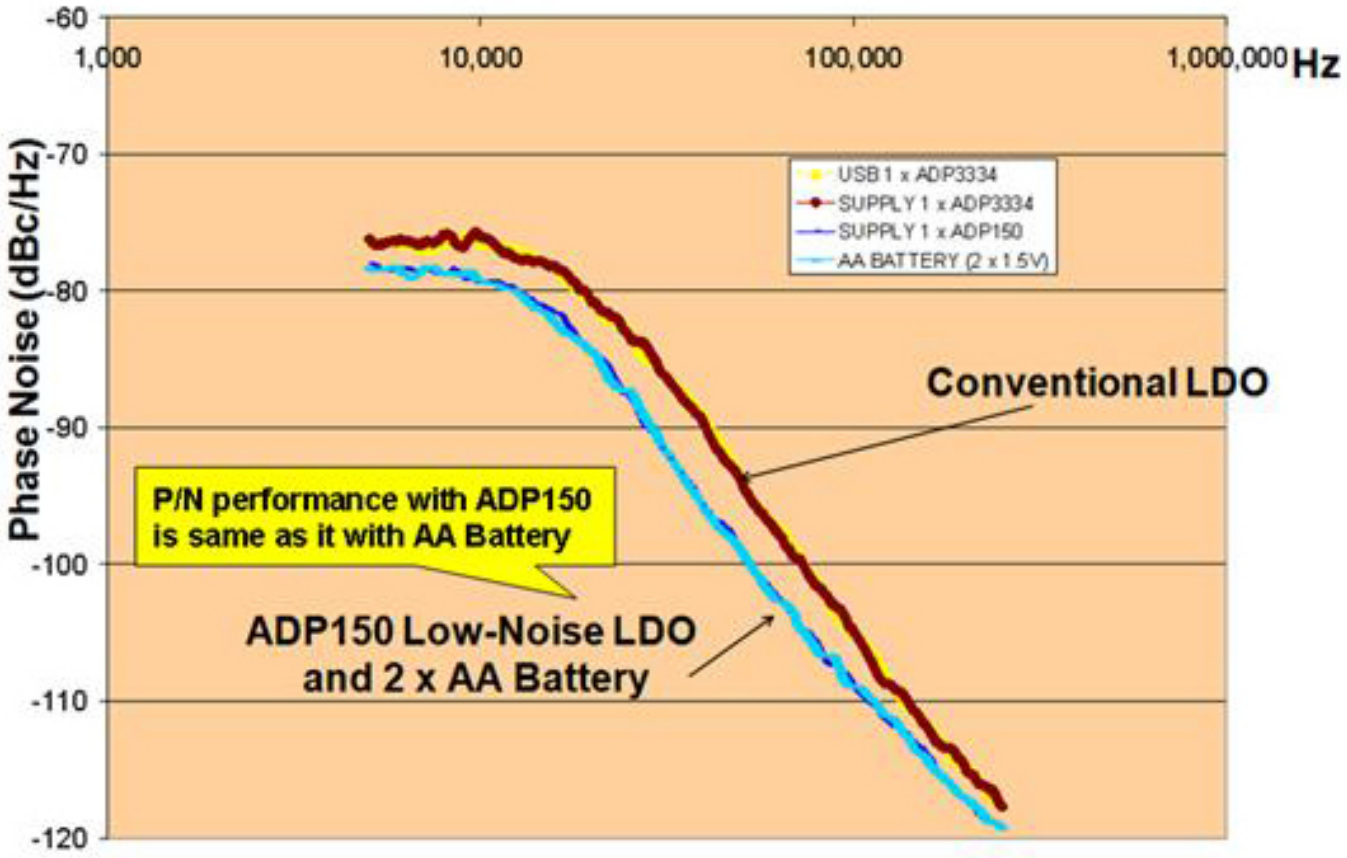

Figure 2. Output noise of conventional LDO, low-noise LDO and AA batteries.

Low noise LDOs provide a major advantage in powering precision analog circuits because they achieve ultra low noise performance even without the necessity of an additional noise bypass capacitor. Analog Devics' ADP150 ultralow noise LDO limits output noise to 9 mV from 10 Hz to 100 kHz and also provides a power supply rejection ratio (PSRR) of 70 dB, making it an appropriate choice for power sensitive analog circuits. Figure 2 shows that the ADP150 provides power at 1/3 the output noise level of a conventional LDO, delivering power that is essentially as clean as an AA battery.

What is the best way to configure low-noise LDOs to power a VCO+PLL? The voltage reduction provided by LDOs is dissipated as heat so thermal considerations are important. Even when one LDO provides sufficient power, thermal considerations often call for the use of multiple devices for thermal management purposes. Below we calculate the temperature rise for the case where just a single LDO is used to power Vvco, Vdd and Vout of the ADF3450A.

For 1 LDO, Vin =5.2 V and Vout =3.3 V. Itot= 79 mA+86 mA =165 mA
Pd = (Vin-Vout) × Itot = (5.2 V – 3.3 V) × 0.165 mA = 0.313 W
Theta JA = 152°C/W
Temp rise = Theta JA × PD = 152°C/W × 0.313 W = 47.65°C
Junction temp = Temp rise + Ambient = 47.65°C + 85°C = 132°C

These calculations were repeated for the case where two or three LDOs are used.

The results are summarized in Table 1.

Number of LDOs	Vvco	Vdd	Vout
1	Temp rise – 47.65°C Junction temp = 85°C + 47.65°C = 132°C		
2	Temp rise = 24.5°C Junction temp = 85°C+24.5°C=109.5°C	Temp rise = 22.8°C Junction temp = 85°C+24.5°C=107.8°C	
3	Temp rise = 24.5°C Junction temp = 85°C+24.5°C=109.5°C	Temp rise = 8.0°C Junction temp = 85°C+8.0°C=93.0°C	Temp rise = 15.0°C Junction temp = 85°C+15.0°C=100.0°C

Table 1: Temperature rise for one, two or three LDOs powering VCO+PLL

Table 1 shows that a single LDO cannot successfully power the VCO+PLL because the LDO's maximum operating junction temperature of 125°C is exceeded by 7°C. Two LDOs, on the other hand, provide acceptable thermal performance by reducing the maximum junction temperature to 109.5°C. The table shows further that adding a third LDO provides no additional thermal benefit because the maximum junction temperature remains at 109.5°C.

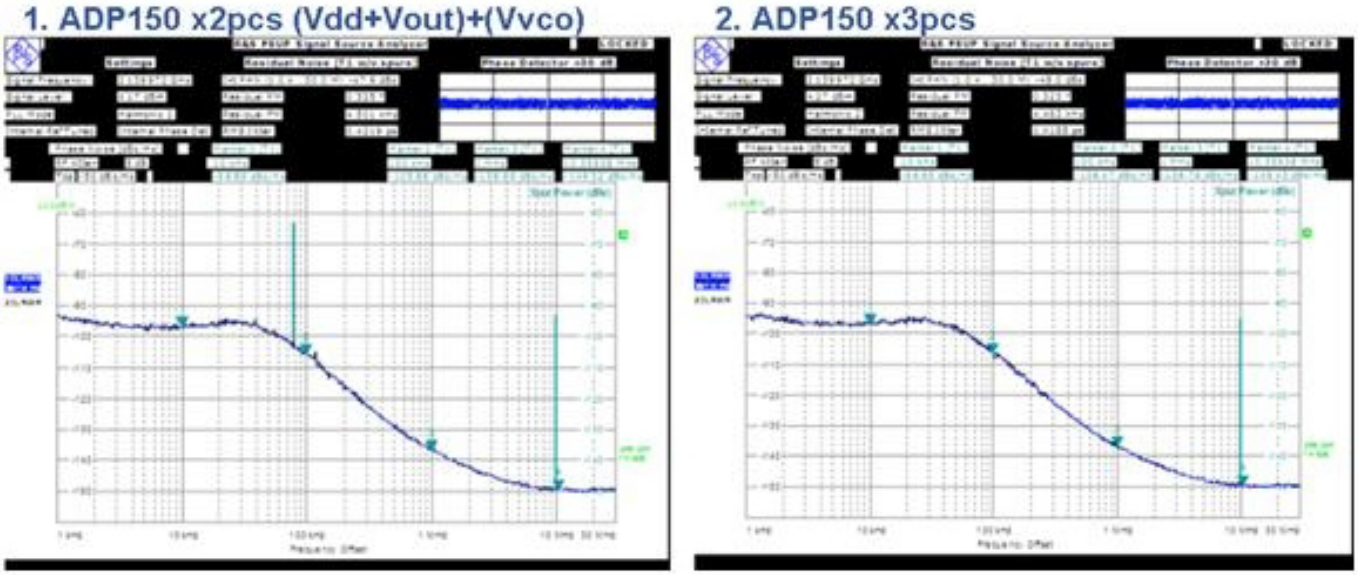

Figure 3. Phase noise comparison of VCO+PLLs powered by two and three LDOs.

Furthermore, Figure 3 shows that noise performance is the same regardless of whether two or three LDOs power the VCO+PLL.

Use of an ultra low noise LDO has a significant impact on passive component selection. Innovative design techniques provide superior noise performance without

the need for an extra bypass capacitor. One such an ultra low noise LDO is optimized for use with tiny 0402 or 0603 1-mF ceramic input and output capacitors to meet the requirements of high performance, space constrained applications.

It's important to note that the effective series resistance (ESR) of the output capacitor affects the stability of the LDO control loop. A minimum capacitance of 1 µF over voltage and temperature with an ESR of 1 Ohm or less is recommended to ensure stability. The transient response to changes in load current is also affected by output capacitance. Use of a larger value of output capacitance improves the transient response of the LDO to large changes in the load current.

Connecting a 1 µF capacitor from VIN to GND reduces the circuit sensitivity to the PCB layout, especially when long input traces or high source impedance is encountered. If output capacitance greater than 1 µF is required, increase the input capacitor to match the output capacitor.

Low noise is important for LDOs used in the analog environment because analog components are more sensitive to noise. The new generation of low noise LDOS use innovative circuit topology to achieve ultra low noise performance, making them ideal for noise-sensitive analog and RF applications. The example shown in this article demonstrates how a low noise LDO can provide a substantial reduction in PLL output phase noise.

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