Three Unique FPGA-based Logic Analyzers – Each Designed in Just One Day

Jake Janovetz, Opal Kelly

A recent engineering design challenge asked FPGA experts to design a "Logic Analyzer in a Day" using off-the-shelf Opal Kelly FPGA-USB modules and its Front Panel SDK. The objective was to showcase the design capabilities of these engineering experts and to demonstrate how quickly, using FPGA modules and software, significant engineering projects can be implemented.

The results? Three different "exhibition quality" logic analyzers, all available, for free, for ECNmag readers to download and use as the starting point for their own FPGA design projects.

The Challenge "Rules"

The rules were flexible to allow the experts to use familiar tools and creative approaches:

- Spend no more than one working day on the project.
- Create the design using an XEM3005 or XEM3010 module and corresponding breakout board.
- Any HDL used must be open-sourced after the challenge.
- Any software created may be any language/platform as long as the source code, or similar, is made available to other users/designers for free.

• Typical logic analyzer features are provided as a guideline, but no firm specification is provided.

The Three Logic Analyzer Designs

The challenge resulted in three different design approaches using two different FPGA modules, two different languages, C# and LabVIEW, and the Opal Kelly FrontPanel SDK. Similar approaches were used for testing signals internally, but three very different approaches were used for generating graphical user interfaces.



extensive experience used a modular approach to design his logic analyzer, leveraging his past designs and tools he had on hand.

Logic Analyzer in a Day -- Design Basics:

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- HDL: VHDL
- Software Language: C# + FrontPanel SDK
- Hardware: Opal Kelly XEM3005 and BRK3005

Rainer was able to pull extensively from previous work and built a very functional graphical logic analyzer. He used the BRK3005 and incorporated a simple pseudorandom signal generator to exercise his logic analyzer. When male headers are installed in the BRK3005, several jumpers connect his signal generator to his logic analyzer to easily demonstrate the capabilities. The user specifies the trigger mechanism using an intuitive 0, 1, or X (don't care) selection next to each signal name and can even set the trigger position within the full capture buffer.

Rainer designed a graphical user interface (GUI) with several special features, including an option to click on one of the signal names and change the name, and the ability to change the associated color in the waveform display. He also included triggering options to initiate the capturing of signals, along with rudimentary Zoom and Scroll features in the display itself.

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Rainer Malzbender, Logic Analyzer in a Day



2) **Kevin Smith**, also a seasoned HDL expert, added excitement to his project by using a language that was new to him—C# under Microsoft Visual Studio. He leveraged knowledge from numerous FPGA-based designs he had created in the past.

Logic Analyzer in a Day -- Design Basics:

- HDL: VHDL
- Software Language: C# + FrontPanel SDK
- Hardware: Opal Kelly XEM3010 and BRK3010

Kevin's analyzer has a simple GUI with textual output of the acquired data rather than a waveform view. Kevin's VHDL has a few hidden gems that could prove useful to other developers, including extensive Python scripts for command-line build of Xilinx projects, as well as a unique way to define endpoints within the FrontPanel framework. Another aspect of Kevin's design is the ability to select and copy the values out of the "Data Sampled" area and paste them into other applications, like Word or Excel. Three Unique FPGA-based Logic Analyzers - Each Designed in Just One Day

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Kevin Smith, Logic Analyzer in a Day



3) **Klaus Zietlow** runs a one-stop shop for electronics design, using analog, digital or mixed signals. Klaus has a fully equipped lab where he works on projects ranging from high-speed, high-precision analog, to FPGA embedded multiprocessor designs, to ultra low-power radios.

Logic Analyzer in a Day -- Design Basics:

- HDL: Verilog
- Software Language: LabVIEW + FrontPanel SDK
- Hardware: Opal Kelly XEM3005 and BRK3005

Klaus is a long-time user of LabVIEW for prototyping complex systems, so it was a natural choice for him to re-use some previous projects as the base for the graphical display of his logic analyzer. Inputs to the logic analyzer were built in a pattern generator. LabVIEW is often used as a platform on which designers build test, measurement, and prototyping systems, so it was a natural platform for the development of Klaus' logic analyzer.



Klaus Zietlow Logic Analyzer in a Day

The 'Logic Analyzer in a Day' Challenge has truly demonstrated how easily and quickly prototype designs can be produced using Opal Kelly's FPGA modules with FrontPanel SDK. It also has provided meaningful, free, 'getting-started' code for other designers to use in their own projects.

All three designers point out that their work is not production quality and has not been through thorough testing and debugging. Rather it is exhibition quality prototype work.

More information and the three designs are available at: <u>http://www.opalkelly.com/experts/logic/</u> [1].

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[1] http://www.opalkelly.com/experts/logic/