The Next Steps in OpenVPX Development

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VPX continues to rapidly grow in military, aerospace, and other applications. Its' combination of high performance, 3U or 6U form factors, IO flexibility, and compatibility with bus architectures such as VME has helped it become the fastest growing platform in the embedded ecosystem. The VPX family of specifications includes VITA 46.0 (core speficiation for VPX), VITA 48 (rugged enhanced chassis/cooling design), and VITA 65 (OpenVPX specification).

OpenVPX is now beginning to sprout promising green shoots as interoperability has become a significant focus around the VPX topic. As this unfolds, the next steps of VPX development are taking root. This includes the use of special connectors for RF systems, the migration to higher Gbps speeds and the inherent signal integrity issues that arise, testing boards and backplanes at multi-Gbps speeds, and the use of advanced cabling solutions.

OpenVPX Background
VPX had been growing at a rapid pace the past few years, however, a significant issue was beginning to emerge. As there was tremendous flexibility in the pinout configurations of VPX, interoperability between vendors was a serious problem. So, OpenVPX was created to define profiles where sets of module, backplanes, and chassis would all work together.

In brief, OpenVPX provides definitions for Backplane Configurations, which are comprised of Slot Profiles, of which various Module Profiles can plug into. The Module and Slot Profiles ensure that a vendor's VPX boards (modules) have pinouts that are interoperable within the VPX backplane slots. The Backplane Configuration tells the user which Slot Profiles are utilized, including information on the data rate, routing topology, and fabric used.

The Backplane Profiles tells us what slot profiles are incorporated, the pitch, and the data rate. The profile name gives us some basic information about the backplane. So, in the 3U Backplane example, this is it's profile name: BKP3-DIS06-15.2.14-1

BKP = backplane
3=3U

DIS = Distributed mesh topology
06=6 slots
15.2.6 = VITA 65 specification section location of this configuration
-1 = 3.125 Gbps

Backplane Topology charts also provide a convenient illustration of the routing configuration for the backplane. See Figure 1.

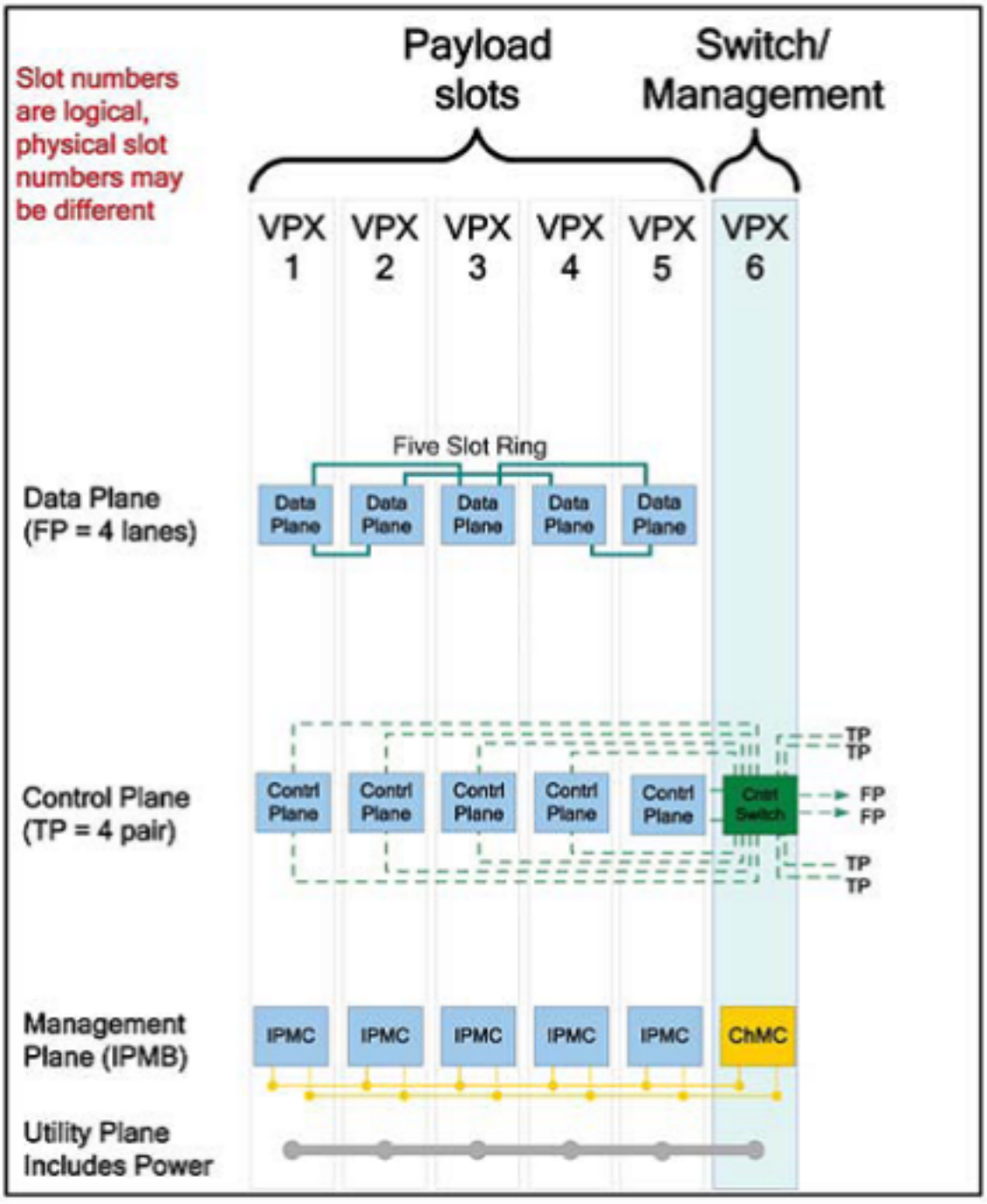
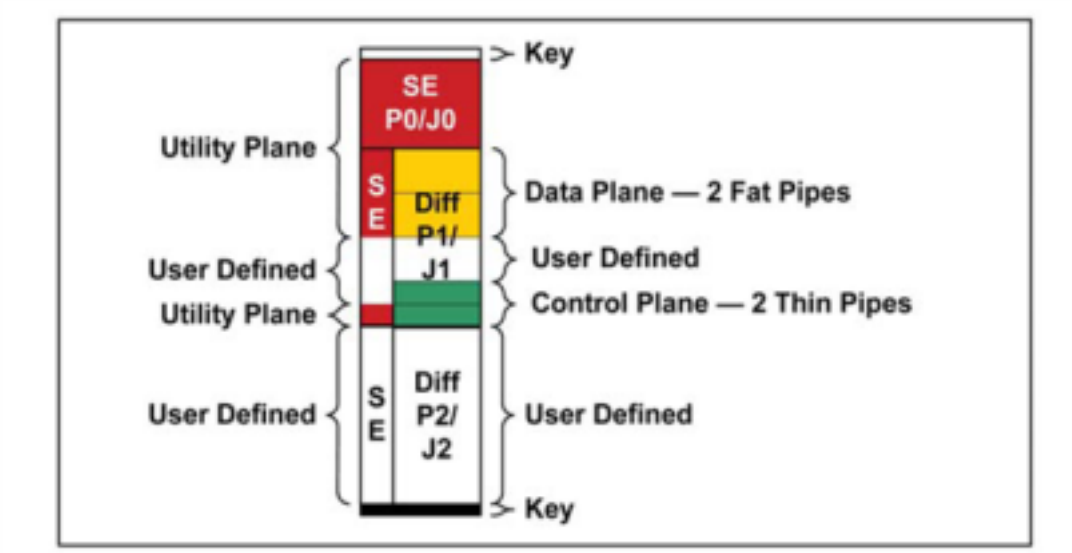


Figure 1: The Backplane Topology diagram shows the Data Plane and Control Plane routing topologies, as well as the Management Plane and Utility Plane configurations.



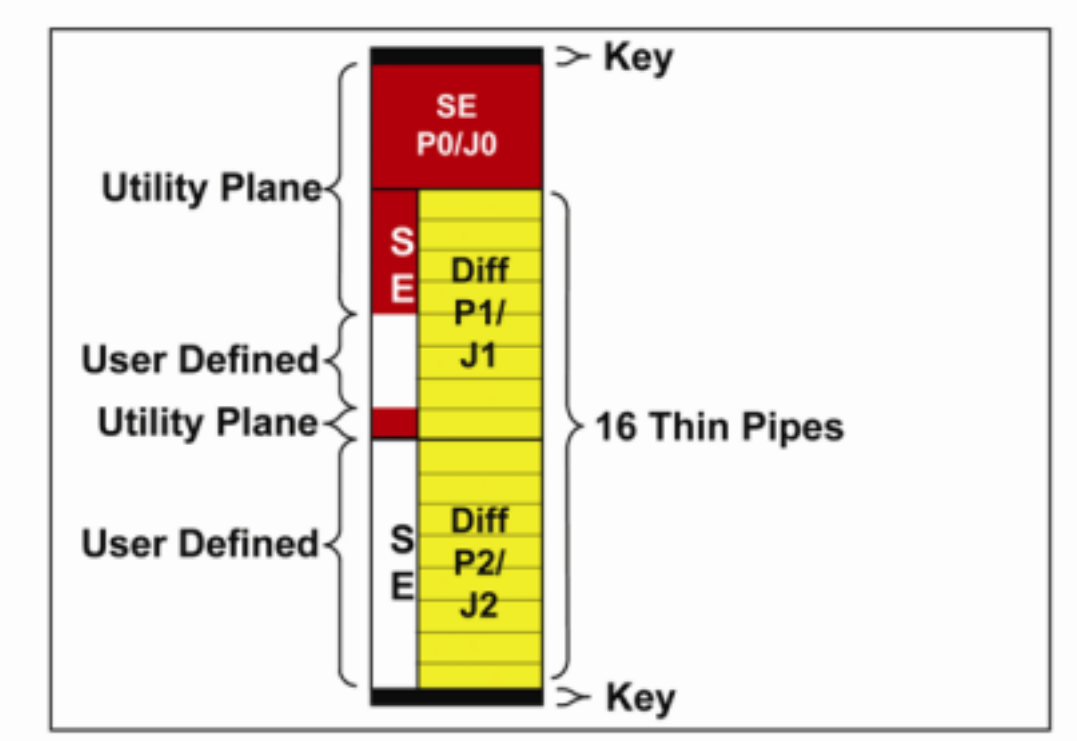


Figure 2a and 2b: The charts show the Payload Slot and Switch Slot profiles respectively. The VITA 65 (OpenVPX) specification includes which Module profiles plug into these slot profiles, ensuring interoperability.

Developing VPX/OpenVPX Systems

In developing VPX systems, the higher data rates will introduce challenges for signal integrity and performance. There are three standard data rates currently called out in the VITA 65 specification. This is the -1, -2, or -3 at the end of the profile name.

-1 = 3.125 Gbps
-2 = 5.0 Gbps
-3 = 6.25 Gbps

As we move to higher speeds, it will be more challenging for designers to meet the performance requirements. So, it’s critical that these systems go through proper signal integrity analysis. For say a BKP3-DIS06-15.2.14-2 backplane at 5.0 Gbps, you could employ pre-design modeling to create the parameters for the design. From there, the simulation studies will tell you if the expected results are within the set guidelines for the design at the speeds given.

Once you design and fabricate the backplane, the post-design characterization studies will determine if the unit you built actually meets the defined performance criteria. The VITA 68 specification is in the works as the Channel Compliance Standard. It’s important that the methodologies are clearly defined for channel compliance. These efforts will help ensure that the industry is comparing apples-to-apples when it comes to signal speeds and SI results.

Using VPX, designers should be mindful that if their labs can handle the testing required for their system. This includes:

• Lab equipment can handle high speed data, including the cables
• The lab queue can meet their desired timeframes for fast turnaround
• The engineers are familiar enough with the VPX specification and design guidelines

Outsourcing this to a third party is always an option. It is recommended that an expert in VPX solutions is chosen. There are also new tools that help designers quickly and efficiently test their prototype systems. One such tool that is available for VPX and other architectures is a SerDes Test Device. The device is used to measure the Bit Error Rate (BER), perform pre-emphasis tuning, and pattern generation. Using VPX cables, the backplane can be tested for VPX systems (or any architecture). See Figure 3 of SerDes Test Device testing a VPX Backplane.

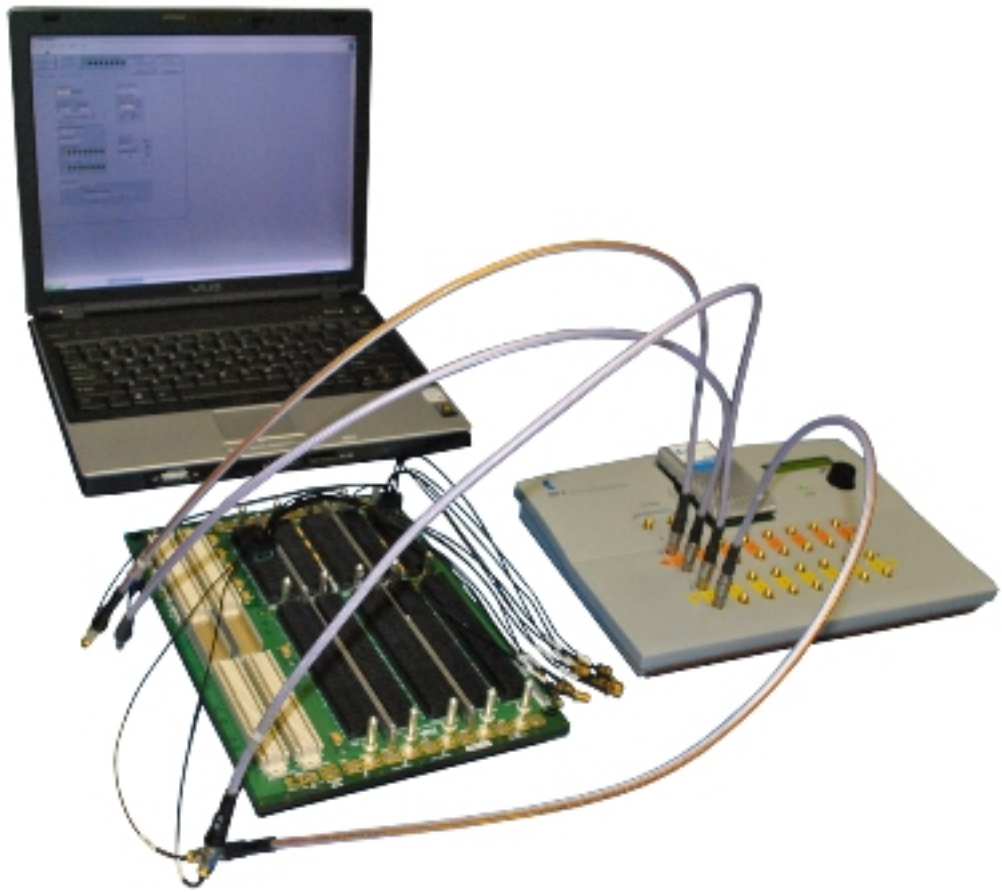


Figure 3: With VPX Cables plugged from the backplane to SMA contacts, the VPX SerDes Test Module can test various signal lines across the backplane, on VPX boards, or the full interconnect path.

Working with the very fast PCI Express, Serial RapidIO, or other serial signals, pre-emphasis tuning can be an important element in ensuring the high-speed performance of a VPX system. Compared to a full laboratory of oscilloscopes, TDRs, etc, the SerDes Test Device is much faster, simpler, and more cost-effective.

Pre-Emphasis Tuning

The SerDes Test Device helps optimize the performance of the system since you can characterize the backplane and configure pre-emphasis settings on VPX boards. To address losses associated with variable backplane trace lengths, new serial transmitters can compensate for backplane losses by controlling parameters such as pre-emphasis and current boost. For example, a typical commercial Serial RapidIO device offers register control for driver strength, supply current, and driver pre-emphasis. By selecting different driver settings on the device, backplane trace losses can be compensated. Figure 4 shows an example of two eye diagrams for a single serial link but with different driver pre-emphasis settings. In the top part of the figure, a closed “eye” is observed, whereas an open “eye” is observed in the bottom part of the figure. In general, closed eyes result in poor system bit-error-rate performance and hence poor aggregate system bandwidth.

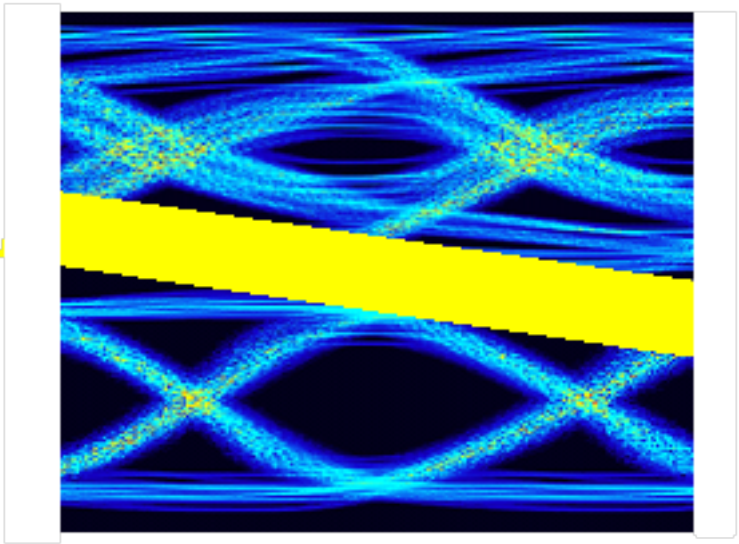


Figure 4: Eye diagrams of a serial link. Top: no pre-emphasis, bottom: optimal pre-emphasis.

VPX Cabling

As described earlier, VPX Cables are now available that plug directly into the MultiGig connector. This is achieved via wafers that snap into the backplane connector. (See Figure 5)

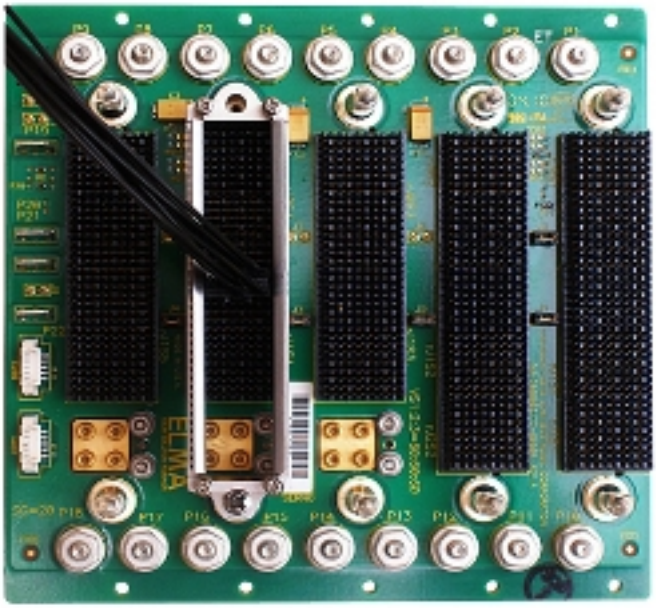


Figure 5: The locking bars are securely holding the wafers in place on the MultiGig connector for this VPX Cabling setup. The cables can be used in both development and deployed applications. Note: There are also gold coax contacts for RF signals.

The cabling system can be used for IO to bulkhead connectors, slot-to-slot connections, and out-of-band communication. The cabling solution can also be used for system development. The direct cabling system also has front-plug versions, which allow testing across the backplane or full interconnect path.

One wafer (essentially a thin pipe) has 4 lines of coax cables so that both differential pairs are terminated. To construct a fat pipe, 4 of the wafers can be

snapped together. Aside from wafer-to-wafer connections, various types of contacts can be employed on the cables such as SMA, coax, RJ-45, Mil C-38999, etc.

The cabling system can also be used in deployed VPX programs. Many applications such as ATRs, may not have RTM options. In some cases, the signal speeds through the RTM are not fast enough. In other designs, the system cannot afford to lose of slot of space to an IO slot. The VPX cabling system provides a rugged and robust alternative with a high-speed connection. To ensure the cables are held properly in place, shrouds are available that latch around the connector and can be bolted down with screws. A locking bar can then snap into place in the shrouds, fixing the wafers/cable solution into place. See Figure 5.

To provide extra security, a stiffener can be used. This is essentially a plastic molded piece that plugs into the connector slots above and below the cables, holding everything tighter into place.

Coming Soon to an OpenVPX/VPX System Near You

Aside from the new testing/development tools described herein, there are also a wide range of backplane/system developments in the works. One of the more interesting efforts is adding RF connectors onto the backplane. Using a coax connector interface, they can be placed in defined areas of the VPX cards and backplane. The use of RF and optical signals are increasingly desired in Mil/Aero embedded systems. An example of the gold coax contacts for the RF signals can be seen in Figure 5.

Full Testing Range

The industry now offers a wide range of development tools for VPX designs.

This includes:
- VPX Load boards – 3U, 6U
- VPX Load boards – 3U, 6U conduction cooled
- VPX Test Backplanes
- VPX Development System
- VPX Extender Boards
- VPX Universal RTM Cards
- VPX Cabling System
- VPX Serdes Test Devices

The test backplane is a helpful development tool for VPX card developers and system integrators. The engineers can power up one or more VPX blades under test and interconnect their J1 fabric connections as they would be interconnected in the target application. Signals can be passed from one slot to the next with high speed interconnecting cables or signals can be introduced or accessed at J1 fabric connector using the MultiGig-to-SMA cable adapters.

The high-speed architecture for VPX creates design and development challenges. With the wealth of new development and testing solutions, designers will quickly and efficiently be able to troubleshoot and address problems that arise.