The ECN Roundtable - Mixed-Signal ICs

This month's question, **"In what area of development do you feel the most progress in mixed-signal ICs will occur?"** was answwed by Raymond Lee of MagnaChip, Stephen Kempainen of National Semiconductor, and John Whalen of Fairchild Semiconductor.

By John Whalen, Business Development Manager, Mobile Products, Fairchild Semiconductors

One area that we see progress in mixed signal ICs will occur in the area of power management. As 3G and 4G mobile device adoption continues to increase in the marketplace, and as device manufacturers work to gain more functionality by adding chips that enable the highly desirable and expansive list of new applications consumers are looking for, it creates the challenge of how to power hungry mixed-signal ICs without draining the battery so quickly the product is useless.

Design engineers are constantly looking at ways to improve power management performance, focusing on three areas that have the most impact – not including the baseband processor and RF transceiver. These areas are the power amplifiers, the display and the applications/graphics processor. These areas contribute greatly to the user experience, but also require designers to find ways to efficiently manage the power in feature-rich mobile devices in order to extend battery life.

There are many ways to improve overall power management performance of mobile handsets and in particular smartphones with both simple and complex techniques. And this is an area we see significant prospects for progress in mixed signal ICs.

By Stephen Kempainen, Strategic Marketing Director, High Speed Products Division, National Semiconductor

Depending on your viewpoint, a mixed-signal IC is a digital chip integrating analog functions for a System-on-a-Chip (SoC), or an analog chip using digital functions to enhance analog performance. For the SoC case, the mixed-signal IC is an all CMOS device in a 45 nm or larger node where the foundry adds active and passive analog functions into the mainstream technology. However, when it comes to analog, bipolar transistors perform better than CMOS because they create less noise, and provide higher bandwidth with higher output impedance. This results in better performance with less power consumption. When analog performance is critical, then BiCMOS processes (combining bipolar and CMOS transistors) have become the mixed-signal technology of choice.

The challenge is to optimize both the bipolar and CMOS transistor performance. The bipolar performance increases by introducing germanium into the process, which gives us SiGe BiCMOS. The germanium increases electron mobility, which has the benefit of increasing the current density and max frequency of the devices. The result is better performing analog that uses less power than the pure CMOS equivalent. Optimizing CMOS digital performance requires shrinking the geometry to enable faster digital state machines that conserve power.

We'll see more progress when chip designers can take greater advantage of SiGe BiCMOS. These innovations will come from developing a consistently repeatable BiCMOS process with analog functions that are accurately modeled and therefore highly predictable. Then designers can create circuits without having to over compensate for process, voltage, and temperature (PVT) variations. This minimal PVT compensation results in even lower power consumption while simultaneously increasing performance in typical analog functions such as cable equalization or data retiming.

In addition to compensating for PVT variations, key areas for circuit design innovation are compensating for electrical parasitic elements. These unavoidable parasitic capacitors, resistors and inductors inhibit a circuit's performance unless the designer can mitigate their effects. But a designer can only do this if the BiCMOS model is accurately predicting these inhibitors. Therefore, it comes back again to making progress in SiGe BiCMOS process development, where controlling and modeling parasitic elements are critical to improving mixed-signal IC performance.

Raymond Lee, VP and Director Display Systems Division, MagnaChip Semiconductor

High-voltage applications is an area which is increasingly in demand in mixed-signal ICs, particularly as it relates to consumer and automotive applications. It inevitably involves integrating special performance criteria, such as narrower transistor pitch, lower off-state leakage current and improved latch-up immunity in the manufacturing process as well as in analog circuit design.

The integration of unique and specialized functions creates an opportunity to add value to and expand the features available for many existing and new mixed-signal products. One example is high-speed serial interfaces for mobile display driver ICs. Tens of digital bus signals can be replaced with just a couple of differential signal pairs using a high-speed SerDes. Delivering Giga-bit data per second for high-resolution displays such as WSVGA, will reduce manufacturing costs, lower overall power consumption by more than 50%, and eliminate extraneous EMI noise.

The functionality of mixed-signal ICs is getting more complicated. Various operating modes and reconfigurable functions are leading to progress in the development of advanced verification methodology for the mixed-signal circuitry. Today, analog design and verification still require manual work in many aspects that result in many errors. Developing a concrete way to describe and verify the behavior of analog circuits will be more demanding. A chip-level verification methodology with higher accuracy and speed for complex analog/digital design is essential and presents another area for IC development.