Analog Front-End Design for ECG Systems using Delta-Sigma ADCs

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Electrocardiogram (ECG) system analog front-end (AFE) devices are typically designed with discrete off-the-shelf components from various semiconductor vendors. The primary components of a traditional discrete ECG AFE include instrumentation amplifiers, operational amplifiers that implement active filters, and analog-to-digital converters (ADCs). This article discusses the characteristics of electrocardiogram (ECG) signals and different front-end approaches for ECG signal acquisition. Also it discusses the tradeoffs between different approaches and the effects on overall system design. The report also includes a description of potential implementations of the optimal front-end architecture.

The ECG signal consists of three main components: the actual (differential) ECG signal, the differential electrode offset, and the common-mode signal.

• The actual differential ECG signal that appears between the electrodes in any lead configuration is limited to ±5 mV in magnitude and 0.05 Hz to 150 Hz in frequency. The magnitude of this actual ECG signal, together with the resolution required from the ECG signal, determines the dynamic range requirement of the front-end. The frequency content of this signal determines the bandwidth requirements of the analog front-end.

• The skin-electrode interface gives an additional differential DC offset of approximately +/-300 mV. This offset must be manipulated such that the signal chain is not saturated. Depending on the system architecture, the offset can either be removed or preserved.

• In addition to these two signals, the human body can pick up large interference signals from power lines, fluorescent lights, and so forth. This interference can manifest itself as either a normal-mode signal or a common-mode signal. Normal-mode interference can be mitigated by a software-implemented, 50-Hz/60-Hz notch filter. Common-mode interference, on the other hand, is generally countered in one of three ways: increasing the isolation of the ground of the front-end electronics from the earth ground as much as possible; increasing the common-mode rejection of the signal processing circuitry (on the order of 100 dB); driving the patient body with an out-of-phase common-mode signal also referred to the right leg drive.

One of the primary specifications of an ECG front-end is the input-referred noise. It is typically specified to be <30 uV peak-to-peak for the entire system over a bandwidth of 150 Hz (IEC60601-2-51,27). Depending on the type of electrodes used, the impedance of the electrodes can be in the order of tens to hundreds of megaOhms. Hence the front-end needs to have a very high-input impedance.

Based on the resolution of the ADC used in the signal chain, there are two distinct approaches to processing the ECG signal. One approach is to use low-noise amplifiers and to gain the input signal significantly (approximately 500), and thus use a low-resolution (approximately 16-bit) ADC. The other approach would be to use a lower gain (approximately 6) and a high-resolution (approximately 24-bit) ADC.

Figure 1 shows a typical discrete ECG analog front-end with sequential sampling using a 16-bit ADC.

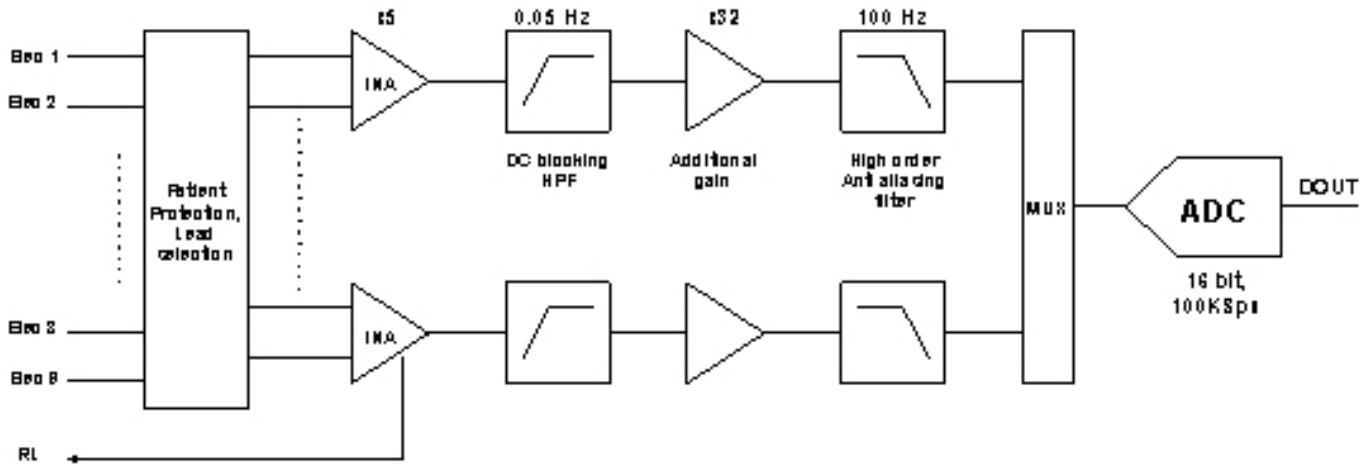

Figure 1. Typical SAR based ECG signal chain with approx values (Sequential sampling).

A typical ADC full-scale voltage is approximately 2.5 V, which implies a gain of 500 (assuming a 5-mV input signal). The total gain is distributed between the instrumentation amplifier (INA) and an additional gain amplifier. Gain is added to the INA in such a way that the electrode DC offset does not saturate the INA. At this point, the DC component must be removed before any further gain can be introduced. Thus, a high-pass filter (HPF) with a corner frequency of 0.05 Hz is added. Once the DC component is removed, the signal is gained up again with another amplifier. This gain stage is followed by an anti-aliasing filter. Nyquist rate converters such as successive approximation register (SAR) ADCs must have a very sharp anti-aliasing filter to avoid aliasing out-of-band noise. Typically, a fourth order or higher active low-pass filter (LPF) is used. The LPF block is followed by a multiplexer block (MUX) that feeds into the ADC.

It can be seen in this type of system that there is a significant amount of analog signal processing that occurs before the signal is digitized, including gain and filtering. Additionally, signal processing in the analog domain limits flexibility. Often, the gain, bandwidth, and DC tracking (that is, baseline wandering) are required to be optimized. Since digital signal processing is relatively lower cost and provides a great deal of flexibility, it is beneficial to move the signal processing to the digital domain. The system described in the next section follows this approach.

Figure 2 shows the same ECG front-end with simultaneous sampling delta-sigma

converters.

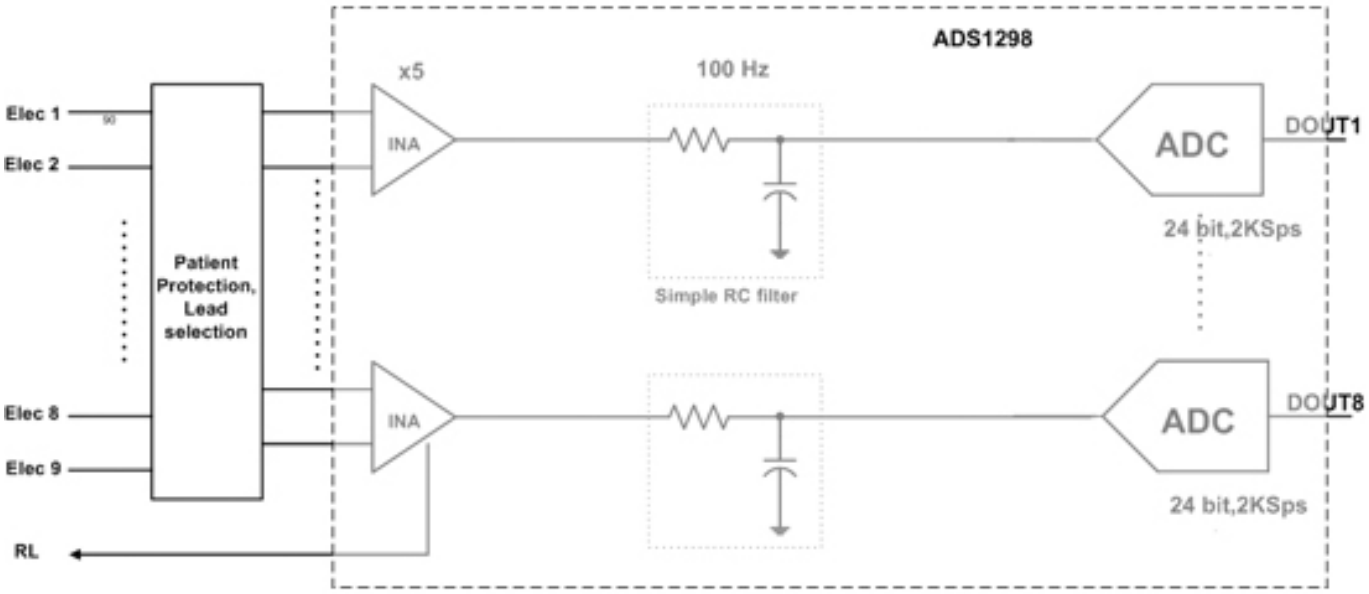

Figure 2. Typical delta-sigma-based ECG signal chain (simultaneous sampling).

Delta-sigma converters are known to give very high-resolution performance using oversampling and noise-shaping principles. By comparing Figure 1 and Figure 2, it can be seen that there is a significant reduction in hardware in the later block diagram. This implies lower cost, size and power. Three blocks (including the high-pass filter, DC blocking filter, gain stage, and a steep, active low-pass filter) are eliminated. Delta-sigma ADCs also significantly relax the anti-aliasing requirements before the ADC. The complicated active anti-aliasing filters, which could require several amplifiers to implement, can be replaced by a simple, single-pole RC filter. The DC blocking high-pass filter is eliminated as well, because the inherent noise of the ADC is significantly lower than the previous solution. In this way, the DC information is not lost, and the various filters can also be implemented digitally. Digital filter implementation also gives the designer flexibility to use adaptive DC removal filters for overall faster response and better rejection of baseline wandering.

One example of a front end using the architecture shown in Figure 2 is the ADS1298 from Texas Instruments. This device provides a low-power single-chip solution for the entire analog front-end. It uses simultaneous sampling low-power delta-sigma converters to achieve the breakthrough combination of size and power, which is critical for portable ECG/EEG applications. Figure 3 shows a 12-lead ECG signal (1mV) acquired from a Fluke simulator using the ADS1298.

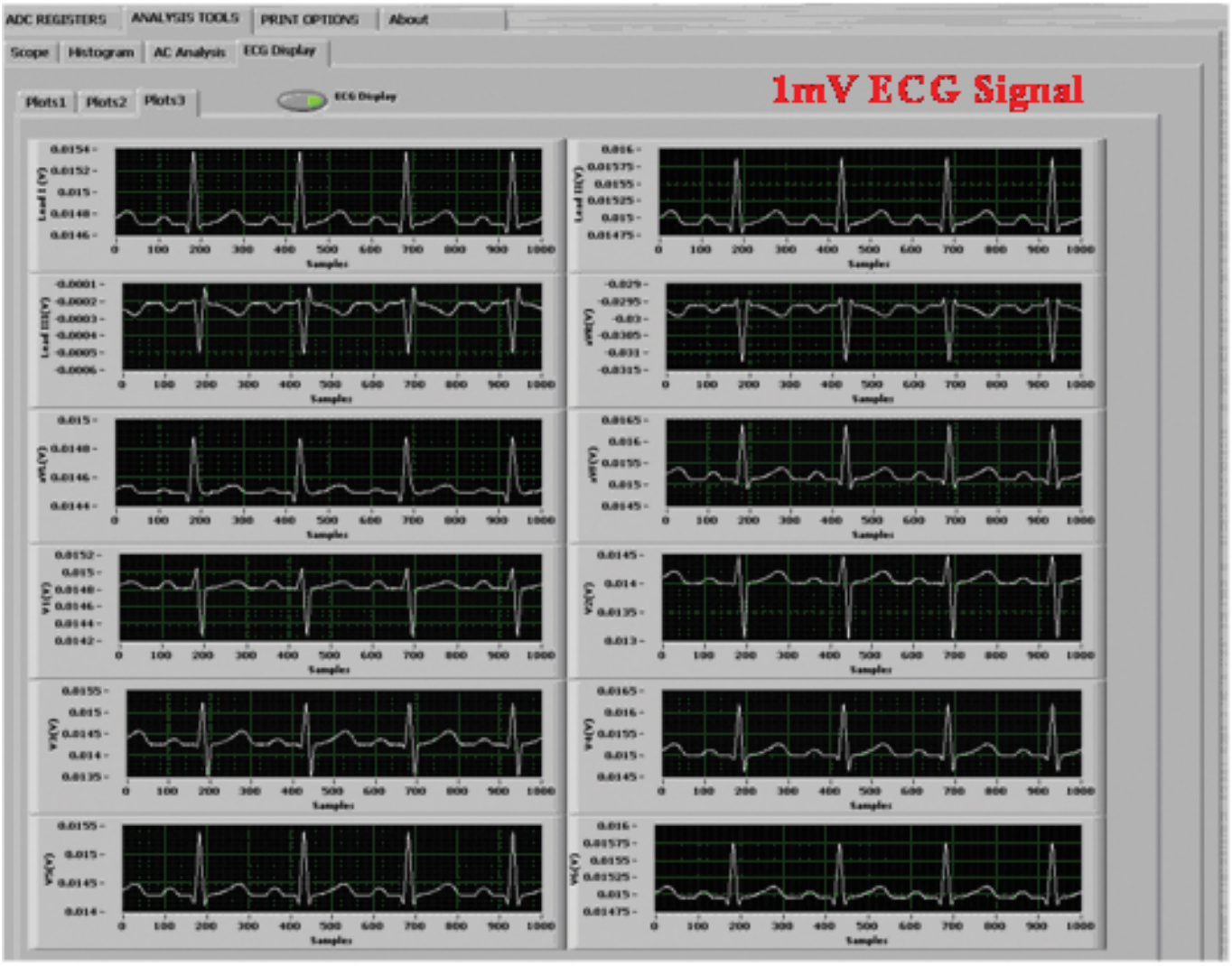

Figure 3. Twelve-lead ECG (6 mW) using simultaneous sampling sigma-delta ADC approach.

Summary

In conclusion, there are several possible front-end approaches to be considered for ECG signal acquisition along with tradeoffs and the effects on your overall system design. Considering the possibilities, using a lower gain (approximately 6) and a simultaneously sampling high-resolution (approximately 24-bit) ADC is optimum with respect to complexity, power and size.

References

• Download a datasheet for the ADS1298 here: www.ti.com/ads1298-ca [1]
• Download an application note here:
• What approach to ECG signal acquisition have you had the most success with? What other challenges are you experiencing? Share your experience and knowledge, explore other ideas, and help solve problems with fellow engineers at the E2E data converter community at www.ti.com/dataconverterforum-ca [2].

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Links:
[1] http://www.ti.com/ads1298-ca
[2] http://www.ti.com/dataconverterforum-ca