Advanced Architecture For DC-DC Buck Regulators Raises The Bar For Conversion Efficiency

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 The emergence of energy-efficiency standards and continued evolution of processing and feature sets to support new products that consumers/enterprises use in everyday life: DVRs, set-top boxes and modems, industrial handhelds, portable media players, bar-code scanners have changed the methodologies employed for addressing DC power conversion, management and distribution. These product designs have traditionally not been as concerned with standby-power dissipation, dynamic load currents, or smaller form factors as for instance – the wireless handset industry. The advent of these challenges in addressing power management solutions is driving a new thinking in the selection of power regulators for powering ASICs, DSP chips, SOCs with core, digital, memory, and IO supplies in these products.

Designers will be looking to leverage the benefits of new high frequency regulator solutions like Fairchild's FAN5354 (3MHZ) Buck regulators, which use state-of-the are design techniques to provide high efficiency over wide load currents (1mA – 3A), significantly lower load transient response and offer very small form factor solutions due to reduced component size and count. Power designers working with these applications, historically have focused more on low cost regulators ICs with <1MHZ switching frequencies where external components are used to ensure soft-start, stability, filtering, and optimization of the load transient response. Until recently, these end markets were not primarily concerned with standby power drain, board space, and the dynamic electrical performance was not critical to meeting system power budgets. In fact, many applications employed inefficient linear regulators up to 3-5A as the power drain was mainly limited by thermal/heat management.

Today's advanced power regulator suppliers like Fairchild are providing solutions that can properly offer relief in addressing these new challenges while still meeting

total noise and error budget specifications with alternative architecture solutions. These new approaches overcome historical concerns over higher frequency regulator topologies (EMI, switching losses, etc) with novel approaches that allow optimization of efficiency and outstanding transient response over a wide operating range. They provide the added advantage of reduced component sizes and cost, advanced IC design optimization, small packaging to achieve smaller total footprint solutions derived from these higher frequency switching topologies.

From an application perspective, the advanced consumer and industrial products that are most in need of these advanced DC -DC switching regulators have the following common challenges to solve:

a) POWER CONSUMPTION (DYNAMIC AND STAND-BY) STANDARDS. Total standby power regulations in Europe and North America are driving <1W average. This effectively requires power designers to find solutions that not only have high efficiency (typically >90%) at full load, but also in load-power states when processing chips, display drivers, memory, I/Os have to be powered in idle-states (to ensure fast response to various features/user requirements) but are not active. This requires DC regulators with very low current drain that is significantly less then system load current during light-load conditions.

b) HIGH PERFORMANCE VIDEO, NETWORKING, DISPLAYS, COMMUNICATIONS. With advanced feature sets offered in products today, some of systems blocks that draw the largest load currents are operating at voltages between 1-5VDC. This includes advanced densely integrated SoC ICs, processor cores for video, displays, digital signal processing, dynamic memory access devices, and high performance communications interfaces like high-speed USB, HDMI as well as a host of new wireless standards (WiFi, LTE, WiMAX, etc.) These cores are based on the industry’s latest high-density 60/45-nm processes that require very low operating voltages (as low as 0.8) VDC but with higher average/peak load currents (1-5A) and very dynamic current consumption (for example a load can shift from 0-3A in as short as 1uS). Due to low-voltage operation the total error budget requirements for proper system operation requires the DC-DC regulator to provide low combined error from drift, ripple, line regulation, and load transient response.

c) SMALLER/THINNER CONSUMER PRODUCT FORM FACTORS. The smaller form factors from board space and thickness profile of higher performance consumer products is challenging system power design teams to find solutions that have the smallest component count and yet utilize smaller components to achieve the same performance. The higher switching frequency topologies lend themselves to reducing inductor size but proper filtering and output capacitance depends on the architecture employed. Applications like set-top boxes, hard disk drives, thin-blade servers and networking cards, medical equipment are adopting aggressive form factors.

So in addressing above challenges, a clear opportunity for divergence exists to leverage these new regulator topologies. Fairchild’s latest product offering - FAN53554 - provides state-of-the-art implementation of these advanced regulator design methodologies.

Consider the requirements for a performance DVR/set-top box device. The figure below shows the typical power budget requirements for the 5 V_{DC} supply rail from offline converter sub-system.

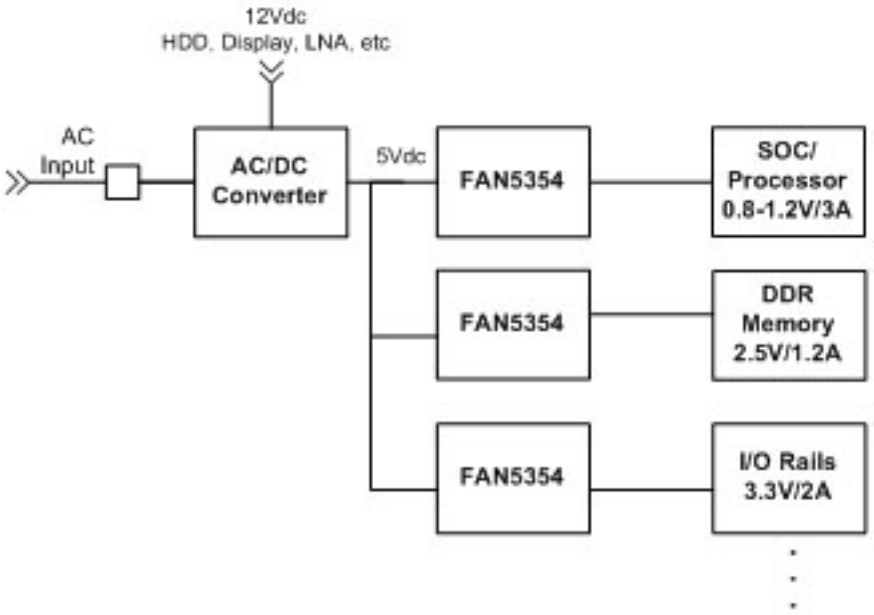

Figure 1: DC 5V Power Demand for Key Blocks in Typical STB/DVR

So in addressing the type of power requirements suggested in the example of Figure 1, FAN5354 is able to address all 3 key power rail requirements with an output voltage that is adjustable from 0.8V to 90% of V_{IN} (V_{IN} max of 5.5V). The device is also able to deliver 3A continuous output current at over 85% and maintain above 80% efficiency with load currents down as low as 2mA. The graph below highlights efficiency vs. load current for VOUT– 3.3V.

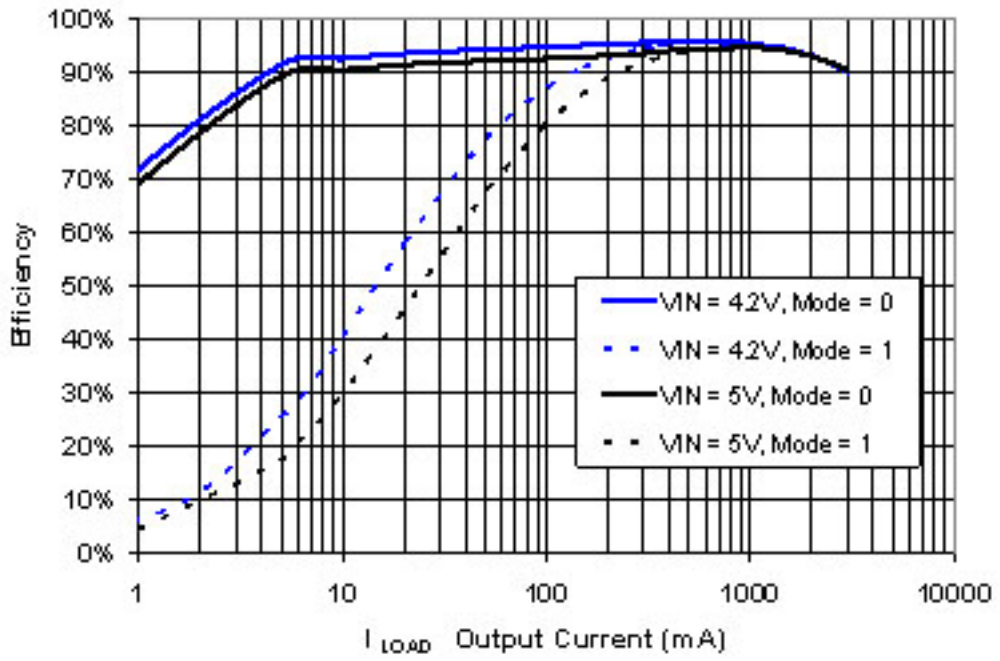

Figure 2. Efficiency vs. I_{LOAD} @ V_{OUT} = 3.3V

This light-load efficiency is obtained as a result of the implementation of automatic transition from PWM (pulse-width-modulation) control at higher load currents (typically >600mA) to PFM (Pulse-Frequency-modulation) modes for lighter-load conditions with a typical quiescent current of 270µA. The device MODE pin can be also controlled to force the device to stay in PWM operation (with degraded light-load efficiency as shown by the dashed curve in Figure 2) or also can be synchronized to an externally-provided PWM signal on the MODE pin. In addressing concerns about audible noise, the minimum PFM frequency is limited to 26kHz to keep spectrum in PFM mode out of the audible frequency range. The architecture also controls the frequency in PWM mode to 3MHz +/- 10%. The ability to controls these parameters provides system designers with knowledge of the expected frequency components of the output spectrum and with the advantage of the higher frequency 3MHz components being easier to filter at the output network.

The other key challenge that power design methodology must consider is meeting total VOUT accuracy and error budget for the regulated supply. A typical standard total error budget is 5% of target VOUT overall operating conditions. This total error budget is a summation of the following key components:

a) DC Output Voltage Over temperature – for most regulators this is trimmed to 1.5% max over operating temperature conditions.

b) Line/Load Regulation – most commercially available regulators have <0.5% for line/load regulation.

c) Ripple Voltage - V_{RIPPLE} is generally related to the switching frequency and parasitics of passive components. The FAN5353 architecture yields performance

that is independent of the output capacitor ESR, allowing for the use of ceramic output capacitors. When driving light loads, the FAN5354 operates in discontinuous current (DCM) single-pulse PFM mode, which produces low output ripple compared with other PFM architectures. The result of this architecture is minimal impact on ripple to the overall error budget. Using for example, a 5V V_{IN}, 1.2V output with 3A load, Figure 3 below provides a typical ripple voltage of 15mV or 1.2%.

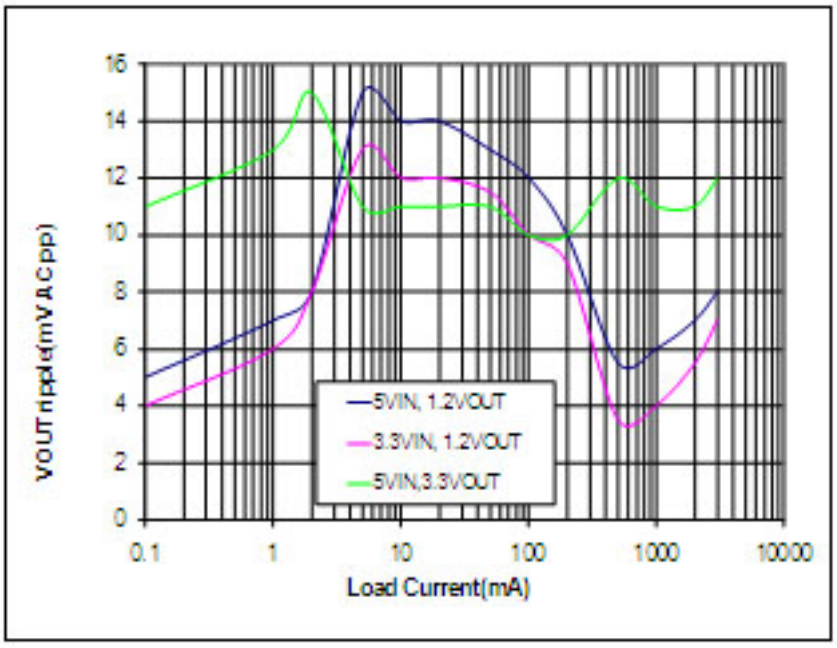

Figure 3: Output voltage ripple vs. load current

d) Transient Response. Since most regulators are trimmed or optimized for above parameters, the only remaining variable in meeting total error budget is load-step transient response. This is where FAN5354 architecture offers significant improvement over conventional solutions. This performance is obtained with unusually small output capacitance (2x10uF 0805-case ceramic capacitors) as well, allowing power designs to meet the specifications without requiring the addition of significant bulk capacitance (and cost) to improve transient response. Figure 4 below shows that for a large load transient step of 1.5A the FAN5354 produces only 30mV of total V_{OUT} error before the regulator tracks out the transient. This represents 2.5% of error and allows for V_{OUT} accuracy to be achieved at low V_{OUT} s in 1-1.8V range.

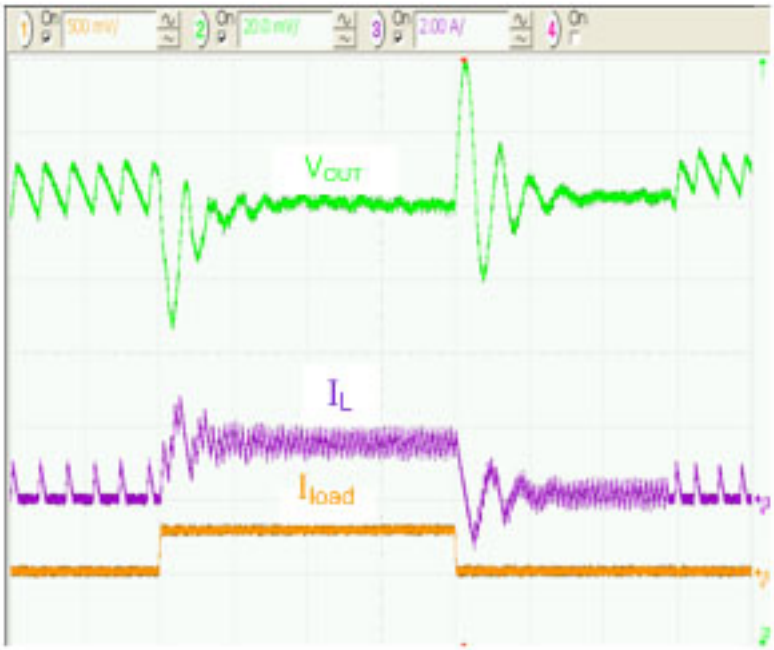

Figure 4. Transient Response load=100mA to 1.5A to 100mA, 5µs/div.

So summarizing the total error budget analysis for our example, it is clear the impact the load transient response of the FAN5354 implementation has on meeting a total 5% error budget window with some margin (about 15%) vs. the limitations of conventional solutions in missing the window significantly especially at low output voltages.

Vin = 5V, Vout = 1.2V, Iload=1.5A				
	FAN5354		Conventional 5V Reg.	
Parameter	% Error	Error, Vdc	% Error	Error, Vdc
DC Accuracy	1.60%	0.0192	1.60%	0.0192
Line/Load	0.25%	0.003	0.25%	0.003
Transient, 1.5A Step	2.50%	0.03	8.33%	0.1
Total Budget	4.35%	0.0725	10.18%	0.1222
Switch Frequency	3MHz		340kHz	
Inductor	470nH		10uH	
Cout to meet Transient Response	2x10uF		2-3x22uF	

Figure 5: Summary of Error Budget Analysis for FAN5354 vs. Conventional Solutions.

Outside of the critical performance metrics discussed, there is also more attention

being paid to board space. As noted above the architectural approach of FAN5354 3MHz solution allows for the user to meet these key specifications while using only two low-cost ceramic output capacitors (offered by a variety of passive suppliers) with smaller capacitance values then conventionally used. This along with the significantly smaller inductor value (470nH) compared with solutions based on legacy 300kHz to 1MHz switching solutions that use inductors in the range of 10-33uH. The FAN5354 is packaged in a small-footprint , MLP 3.5 x 3mm surface-mount packaging that is widely used in applications of this type due to the electrical characteristics and excellent thermal performance – allowing the device to source significant current over wide operating conditions. And lastly, the device has integrated soft-start and internal compensation requiring no additional external components to achieve these functions. The result of smaller inductor, reduced C_{OUT}, minimal external passives, and advanced package solutions is an optimized layout that can fit on <65mm2 board area.

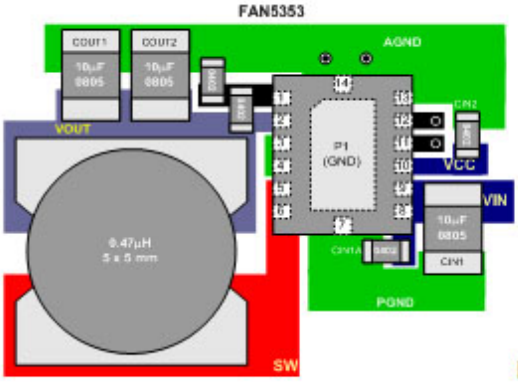

Figure 6: Optimized Board Layout Achieves <65 mm² with 5x5 mm inductor.

The recommended external components are included below:

Component	Description	Vendor	Parameter	Min.	Typ.	Max.	Units
L1	470nH nominal	Vishay IHLP1616ABER47M01 Coiltronics SD12-R47-R TDK VLC5020T-R47N MURATA LQH66PNR47NT0	L		0.47		µH
			DCR		20		mΩ
C_{OUT}	2 pieces 10µF, 6.3V, X5R, 0805	GRM21BR60J106M (Murata) C2012X5R0J106M (TDK)	C	8	10.0	12.0	µF
C_{IN}	10µF, 6.3V, X5R, 0805						
C_{IN1}	10nF, 25V, X7R, 0402	GRM155R71E103K (Murata) C1005X7R1E103K (TDK)	C		10		nF
C_{VCC}	4.7µF, 6.3V, X5R, 0603	GRM188R60J475K (Murata) C1608X5R0J475K (TDK)	C	3.0	4.7	5.6	µF
R3 *	Resistor: 1Ω 0402	any	R		1		Ω

Given the challenges a variety of end markets face in achieving compliance with energy conservation standards with wider scope of coverage, providing power to higher performance chipsets to provide state-of-the art video and digital processing, and fitting solutions into smaller footprint solutions with reduced profiles; the availability of these new regulator topologies comes at an ideal time. The merits demonstrated by Fairchild's advanced FAN5354 DC/DC buck switching regulator in this article highlight the merits of the tradeoffs and optimizations made in order to tailor advanced regulator solutions to these dynamic problems. The continued

evolution of this methodology will enable further advancements in consumer and industrial products sure to come.

For further information please view the datasheet and design information at:
www.fairchildsemi.com/ds/FAN5354 [1]
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