Power Management Design for Portable and Battery Powered Systems

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Integrating the maximum number of functions plus power management into the main chipset for portable, battery powered devices such as mobile phones with capability such as MP3, Mpeg4, and TV, would seem to be critical if an acceptable length of battery life is to be achieved.

Set against this is a contradictory desire from OEMs not to adopt a fully integrated approach. This is due to the potential poor flexibility and long development cycle times of integrated ICs and chipsets when compared to the rapid rate at which new handset designs evolve. Added to this is the fact that fully integrated ICs can stifle end product uniqueness therefore making it difficult for manufacturers to differentiate their products from those of competitors.

Highly efficient, small DC-DC converters and power sub- system ICs may hold the answer to this challenge.

Whether to integrate

Nowadays, portable applications are integrating more and more functions. The general trend pushes handsets to become not only mobile phones, but also digital still cameras (DSC), mobile TV terminals and gaming consoles. Now, digital technology allows application processors to be powerful enough to provide these functions to the end customer.

Communication capability has become critical for the fast download of video and music to the handset. Consumers have become reluctant to connect their handsets to a base station (laptop or desktop computer), and so wireless download has become important. Therefore, more RF modules are being embedded in new handset designs; not only CDMA – GSM and derivatives, but also Wi-Fi, Bluetooth and WiMax.

An increasing feature set is achieved at the price of higher power consumption. With very slow battery capacity and technology improvement, engineers are facing two main challenges. First of all, they have to accommodate the high level of integration of many functions and secondly, they have to provide users with a piece of equipment that has long battery life. To complicate matters further, it is important that the overall form factor of the finished design does not grow in line with the increasing features. Consumers do not want to sacrifice battery life or compactness when enjoying the rich features offered on the latest handsets.

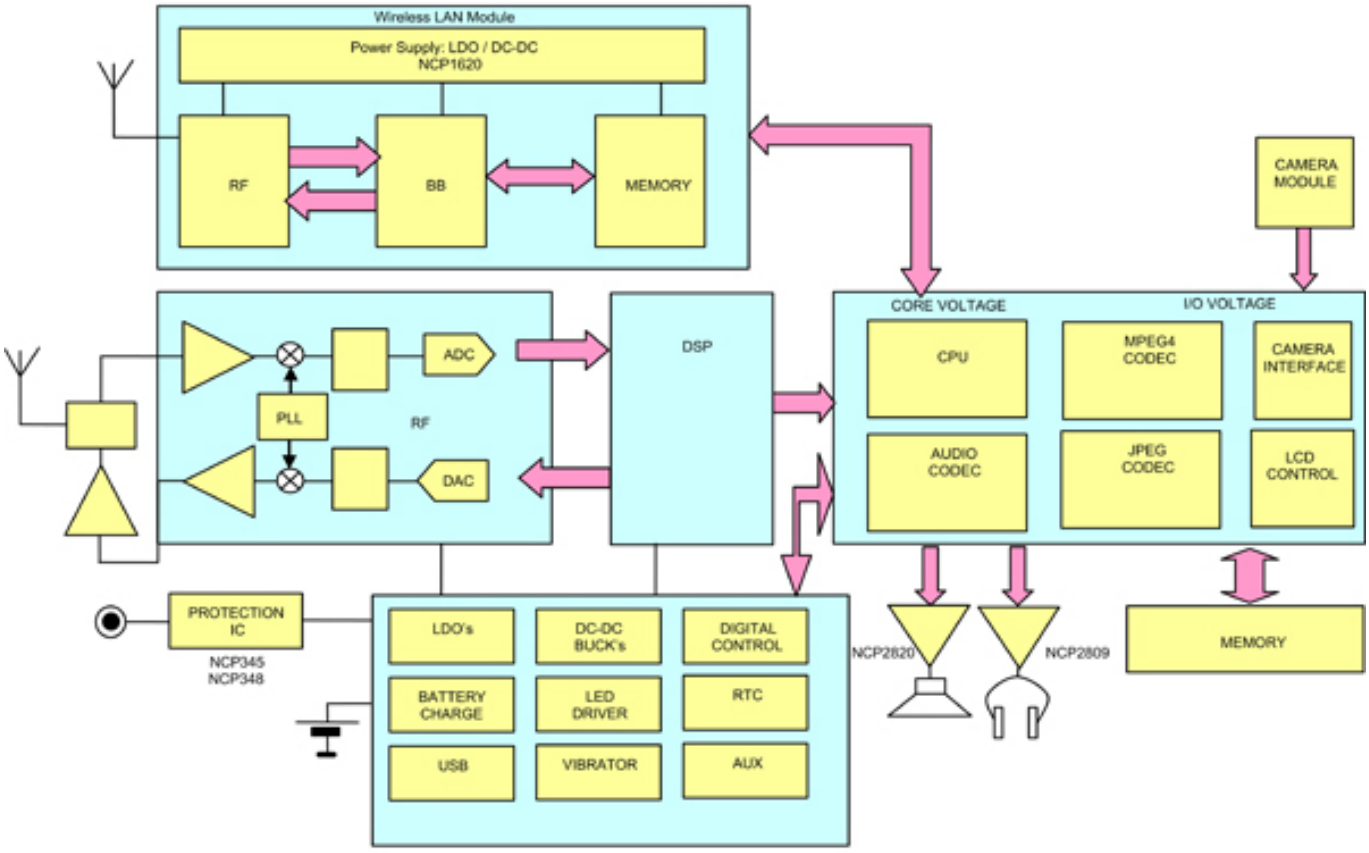

Figure 1: Communicating Handset System Block Diagram

To address these challenges, the best strategy is to integrate more and more functions in the main chip set, resulting in a two or three chip solution with an integrated power management IC (PMIC). Besides providing the power to the handset, the PMIC may integrate all analog functions required, such as the battery charger, USB OTG transceiver, audio signal processing and amplification, plus white LED drivers, comparators, and power drivers for keyboard illumination. This approach simplifies the design and minimizes the resources required to control the power (only one two wires I2C-Bus can control the whole PMU), as well as keeping form factor and economic constraints under control. Despite the benefits of an integrated PMIC, the demand for less integration has increased in the latest generation of handsets.

One of the reasons for this is that using a standard integrated solution will drive the handsets towards becoming standard devices with standard functions. This does not

appeal to those consumers who continually seek to have the latest equipment with the latest features. But, more importantly, this approach hampers OEMs who are seeking to differentiate their products with special features that are not integrated in the basic chip set, and may require an additional application processor and place extra demands on the power supply system.

Another factor that can explain the demand for less integration is development cycle time. On one hand, demand from consumers is pushing the development cycle time to be faster; while on the other hand, the development of a chipset integrating these new functions may take several years. In this market, engineers will not wait for new chipsets and will instead select standalone ICs and application processors.

In order to achieve an effective power supply design, engineers should follow several steps that will lead to the selection of the appropriate power supply architecture and ICs. The entry point for this “top-down” process is the functions that should be embedded in the handset.

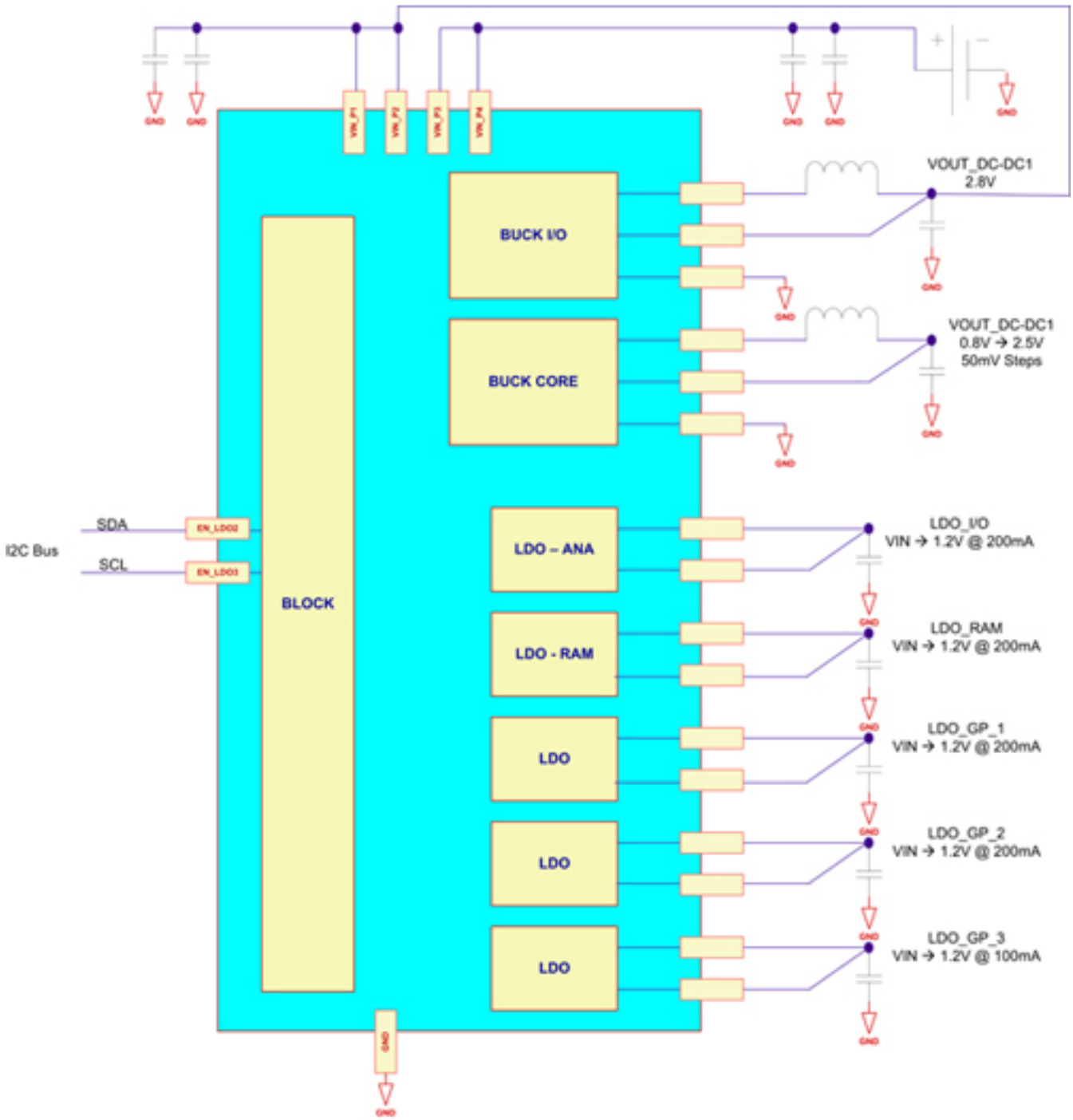

Figure 2: Power Sub-System IC for Application Processor Example

Determining Power Domains

Despite handsets being more feature rich most the functions are usually powered off or in sleep mode. By determining when and why each function should be powered on, designers can define power domains.

Depending on the level of power management required in the application, each power domain may then be divided into different 'sub-power domains'. Ultimately, this important design stage will result in determining what are the different and independent power supply regulators required to operate the handset.

Determining the Voltage Regulators
Determining the voltage regulators is relatively straightforward. For each level of granularity determined during the previous stage, designers need to select either a switching DC-DC converter or a Low Dropout Regulator (LDO).

For power hungry application processor cores, the engineer will have no other choice than inductor based DC-DC converters. They combine more than 90% efficiency with low heat dissipation, small size and a low external component count. Analog Vcc for RF or noise sensitive functions may still require a low noise LDO.

Determining Advanced Power Management Functions
The supply current of processor cores varies with the clock frequency and with the voltage. Neglecting the DC leakage currents, the power dissipation approximation is given by (C = capacitance switched / clock cycle, V = voltage, f = frequency). Although this is not strictly exact because integrated chips do not use only CMOS, the dissipated power decreases quadratically with the voltage and linearly with the frequency. This simple formula leads to define the Dynamic Voltage Scaling (DVS) and Dynamic Frequency Scaling (DFS) techniques.

DVS technique is very effective. However, it requires very accurate voltage regulation with very fine resolution as well as smooth transition from one voltage level to the other. Three percent accurate power supply rails are necessary to achieve good DVS performance.

DVS requires on chip measurement of the digital core burden which is used as closed loop to the PMIC to adjust the power supply voltage. This allows the digital core to operate at the optimal voltage and minimizes the switching losses.

Right now, DVS is not very popular. One of the main reasons is that it drastically increases software complexity. So, the equation between design complexity and battery lifetime improvement has no obvious solution. However, as long as the technology improves, all necessary measurements are more and more embedded and micro coded on chip. Then, complexity is no longer an obstacle for this technique to be more widely adopted.

The power management ICs that will support this technique will be more and more specialized as they need to be designed according to the processor they supply.

Determining the Structure of the Power Management Function
The main chipset for a handset device will comprise a two or three device highly integrated solution with complex PMU. In addition to this main PMU, the power domains and power supply granularity determined during the power management structure definition as well as the advanced power supply options selected by the engineers, may lead to a choice of different power management sub-system ICs for either individual devices or shared by a group of application processors.

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